LEADING AT THE EDGE

TECHNOLOGY AND MANUFACTURING DAY

MOORE'S LAW LEADERSHIP

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DISCLOSURES

Intel Technology and Manufacturing Day 2017 occurs during Intel's "Quiet Period," before Intel announces its 2017 first quarter financial and operating results. Therefore, presenters will not be addressing first quarter information during this year's program.

Statements in this presentation that refer to forecasts, future plans and expectations are forward-looking statements that involve a number of risks and uncertainties. Words such as "anticipates," "expects," "intends," "goals," "plans," "believes," "seeks," "estimates," "continues," "may," "will," "would," "should," "could," and variations of such words and similar expressions are intended to identify such forward-looking statements. Statements that refer to or are based on projections, uncertain events or assumptions also identify forward-looking statements. Such statements are based on management's expectations as of March 28, 2017, and involve many risks and uncertainties that could cause actual results to differ materially from those expressed or implied in these forward-looking statements. Important factors that could cause actual results to differ materially from the company's expectations are set forth in Intel's earnings release dated January 26, 2017, which is included as an exhibit to Intel's Form 8-K furnished to the SEC on such date. Additional information regarding these and other factors that could affect Intel's results is included in Intel's SEC filings, including the company's most recent reports on Forms 10-K, 10-Q and 8-K reports may be obtained by visiting our Investor Relations website at www.intc.com or the SEC's website at www.sec.gov.

KEY MESSAGES

- Intel leads the industry in introducing innovations that enable scaling
- Hyper scaling on Intel 14 nm and 10 nm provides better-than-normal scaling while continuing to reduce cost per transistor
- Intel's 14 nm technology has ~3 year lead over other "10 nm" technologies with similar logic transistor density
- Intel's 10 nm technology provides industry-leading logic transistor density using a quantitative density metric
- Enhanced versions of 14 nm and 10 nm provide improved performance and extend the life of these technologies

Moore's Law is alive and well at Intel

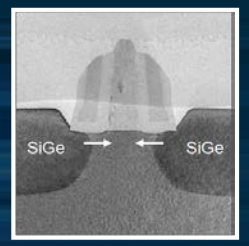
Source: Amalgamation of analyst data and Intel analysis, based upon current expectations and available information.

INTEL INNOVATION LEADERSHIP

Intel leads the industry by at least 3 years in introducing major process innovations

Source: Intel

INTEL INNOVATION LEADERSHIP



Strained Silicon

Intel	90nm		65nm		45nm		32nm		22nm		14nm			10nm		
Year	'03	'04	'05	'06	'07	'08	'09	'10	'11	'12	'13	'14	'15	'16	'17	'18	'19	'20
Others		90nm			65nm		40nm		28nm		20nm		16nm		10nm			

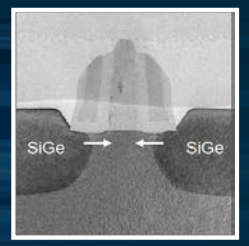
Strained Silicon

>3 years later

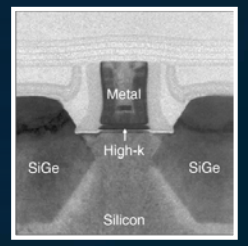
Intel leads the industry by at least 3 years in introducing major process innovations

Source: Intel

INTEL INNOVATION LEADERSHIP



Strained Silicon



High-k Metal Gate

Intel	90nm		65nm		45nm		32nm		22nm			14nm			10nm			
Year	'03	'04	'05	'06	'07	'08	'09	'10	'11	'12	'13	'14	'15	'16	'17	'18	'19	'20
Others		90nm			65nm		40nm		28nm			20nm		16nm	10nm			

Strained Silicon

>3 years later

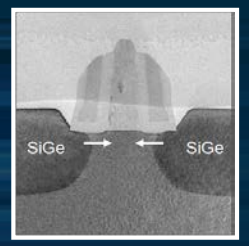
High-k Metal Gate

>3 years later

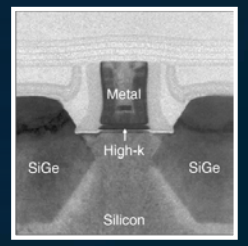
Intel leads the industry by at least 3 years in introducing major process innovations

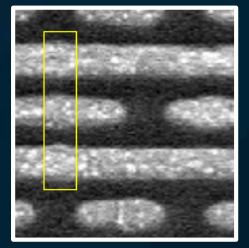
Source: Intel

INTEL INNOVATION LEADERSHIP



Strained Silicon





High-k Metal Gate

Self Align Via

Intel	90nm		65nm		45nm		32nm		22nm			14nm			10nm			
Year	'03	'04	'05	'06	'07	'08	'09	'10	'11	'12	'13	'14	'15	'16	'17	'18	'19	'20
Others		90nm			65nm		40nm		28nm			20nm		16nm	10nm			

Strained Silicon — >3 years later

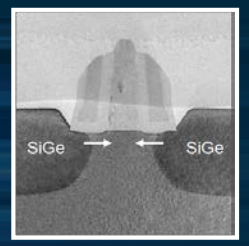
High-k Metal Gate — >3 years later

Self Align Via — >3 years later

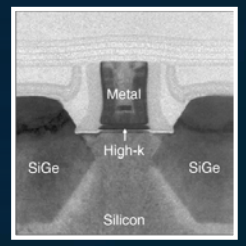
Intel leads the industry by at least 3 years in introducing major process innovations

Source: Intel

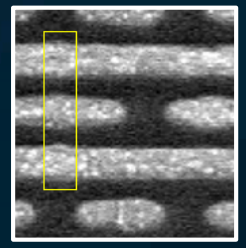
INTEL INNOVATION LEADERSHIP



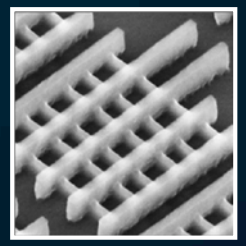
Strained Silicon



High-k Metal Gate



Self Align Via



FinFET Transistor

Intel	90nm		65nm		45nm		32nm		22nm			14nm			10nm			
Year	'03	'04	'05	'06	'07	'08	'09	'10	'11	'12	'13	'14	'15	'16	'17	'18	'19	'20
Others		90nm			65nm			40nm			28nm			20nm			16nm	10nm

Strained Silicon — >3 years later

High-k Metal Gate — >3 years later

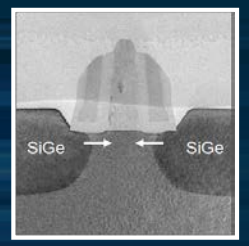
Self Align Via — >3 years later

FinFET Transistor — >3 years later

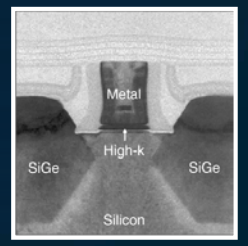
Intel leads the industry by at least 3 years in introducing major process innovations

Source: Intel

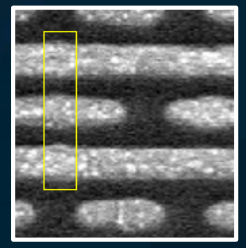
INTEL INNOVATION LEADERSHIP



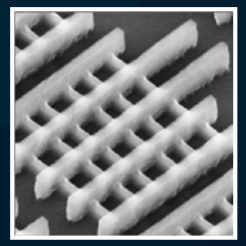
Strained Silicon



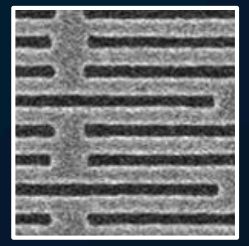
High-k Metal Gate



Self Align Via



FinFET Transistor



Hyper Scaling

Intel 90nm 65nm 45nm 32nm 22nm 14nm 10nm

Year '03 '04 '05 '06 '07 '08 '09 '10 '11 '12 '13 '14 '15 '16 '17 '18 '19 '20

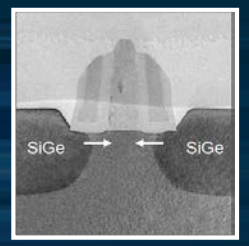
Others 90nm 65nm 40nm 28nm 20nm 16nm 10nm

Strained Silicon	High-k Metal Gate	Self Align Via	FinFET Transistor	Hyper Scaling
>3 years later	>3 years later	>3 years later	>3 years later	~3 years later

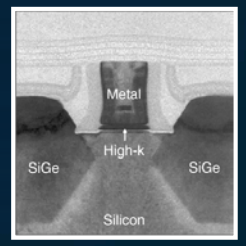
Intel leads the industry by at least 3 years in introducing major process innovations

Source: Intel

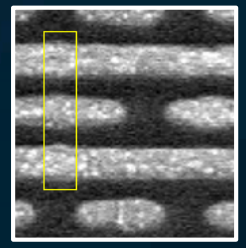
INTEL INNOVATION LEADERSHIP



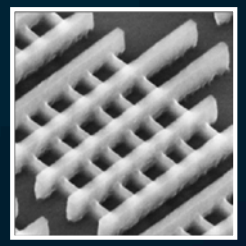
Strained Silicon



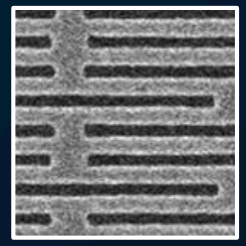
High-k Metal Gate



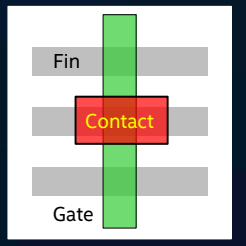
Self Align Via



FinFET Transistor



Hyper Scaling



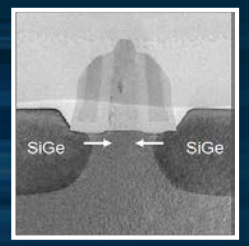
Hyper Scaling

Intel	90nm		65nm		45nm		32nm		22nm		14nm		10nm					
Year	'03	'04	'05	'06	'07	'08	'09	'10	'11	'12	'13	'14	'15	'16	'17	'18	'19	'20
Others		90nm			65nm		40nm		28nm		20nm		16nm		10nm			
					Strained Silicon				High-k Metal Gate		Self Align Via		FinFET Transistor		Hyper Scaling		Hyper Scaling	
					>3 years later				>3 years later		>3 years later		>3 years later		~3 years later		??	

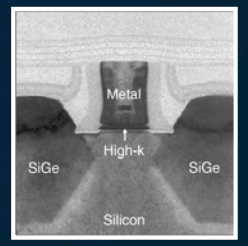
Intel leads the industry by at least 3 years in introducing major process innovations

Source: Intel. 10 nm is based upon current expectations and available information.

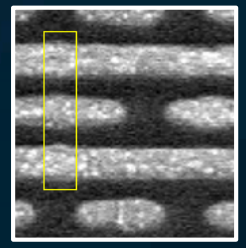
INTEL INNOVATION LEADERSHIP



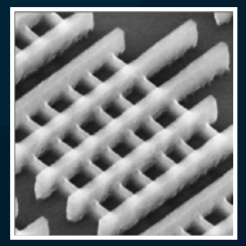
Strained Silicon



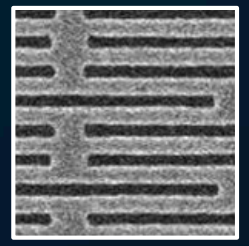
High-k Metal Gate



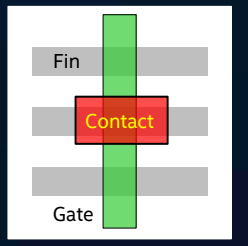
Self Align Via



FinFET Transistor



Hyper Scaling



Hyper Scaling

Intel	90nm		65nm		45nm		32nm		22nm		14nm			10nm				
Year	'03	'04	'05	'06	'07	'08	'09	'10	'11	'12	'13	'14	'15	'16	'17	'18	'19	'20
Others		90nm			65nm			40nm		28nm		20nm		16nm		10nm		
					Strained Silicon					High-k Metal Gate		Self Align Via		FinFET Transistor		Hyper Scaling		Hyper Scaling
					>3 years later					>3 years later		>3 years later		>3 years later		~3 years later		??

Intel developed all the major logic process innovations used by our industry over the past 15 years

Source: Intel. 10 nm is based upon current expectations and available information.

INDUSTRY RECOGNITIONS

2008 SEMI AWARD FOR NORTH AMERICA

"For integration of strain-enhanced mobility techniques for CMOS transistors"

2012 SEMI AWARD FOR NORTH AMERICA

"For the first development, integration and introduction of a successful high-k dielectric and metal electrode gate stack for CMOS IC production"

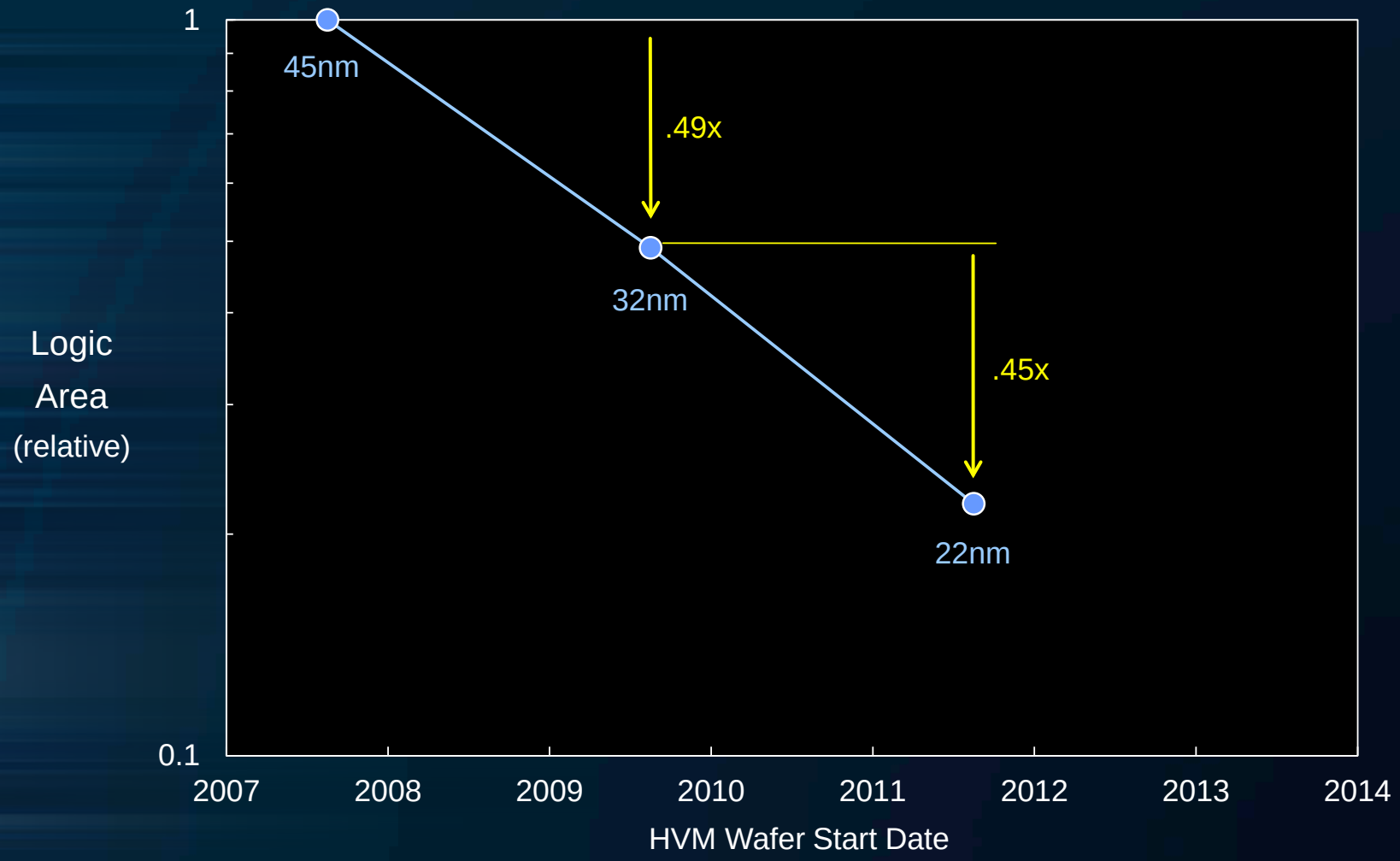
2015 SEMI AWARD FOR NORTH AMERICA

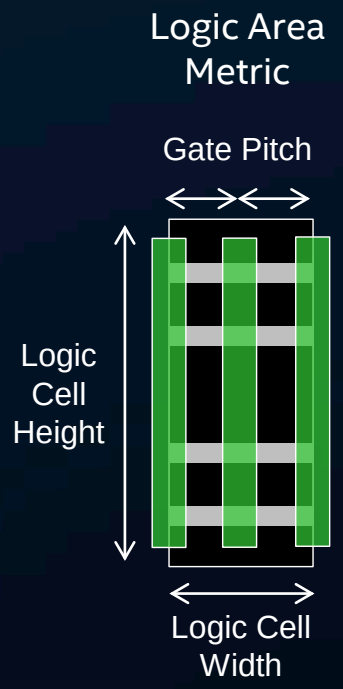
"For implementation of bulk CMOS FinFET production"

2016 IEEE CORPORATE INNOVATION AWARD

"For pioneering the use of high-k metal gate and tri-gate transistor technologies in high-volume manufacturing"

LOGIC AREA SCALING

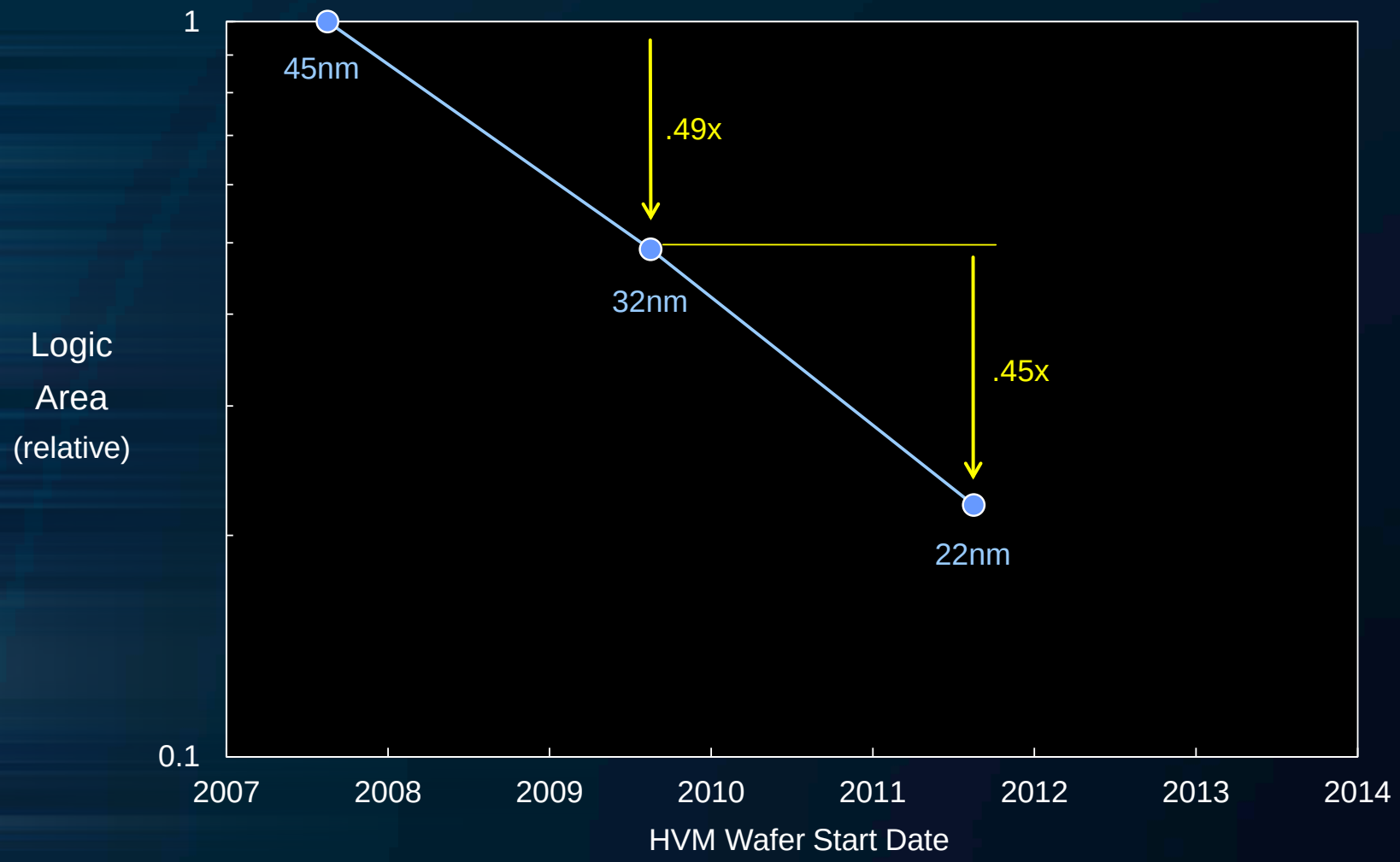


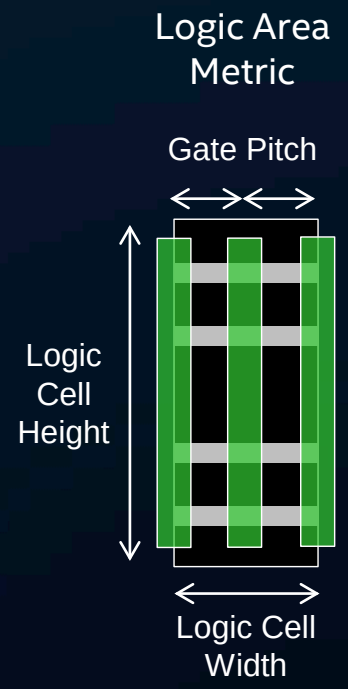


Traditional logic area scaling was ~0.49x per generation using a "gate pitch x cell height" metric

Source: Intel

LOGIC AREA SCALING

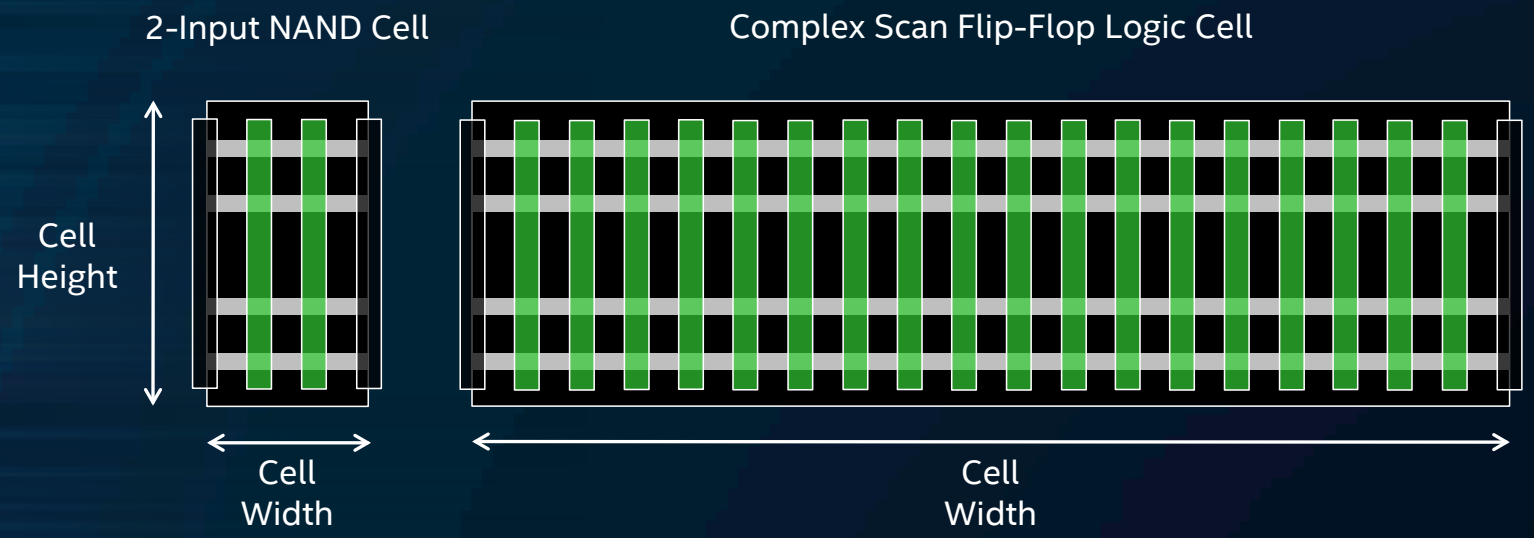




… but "gate pitch x cell height" is not a comprehensive transistor density metric

Source: Intel

LOGIC TRANSISTOR DENSITY METRIC

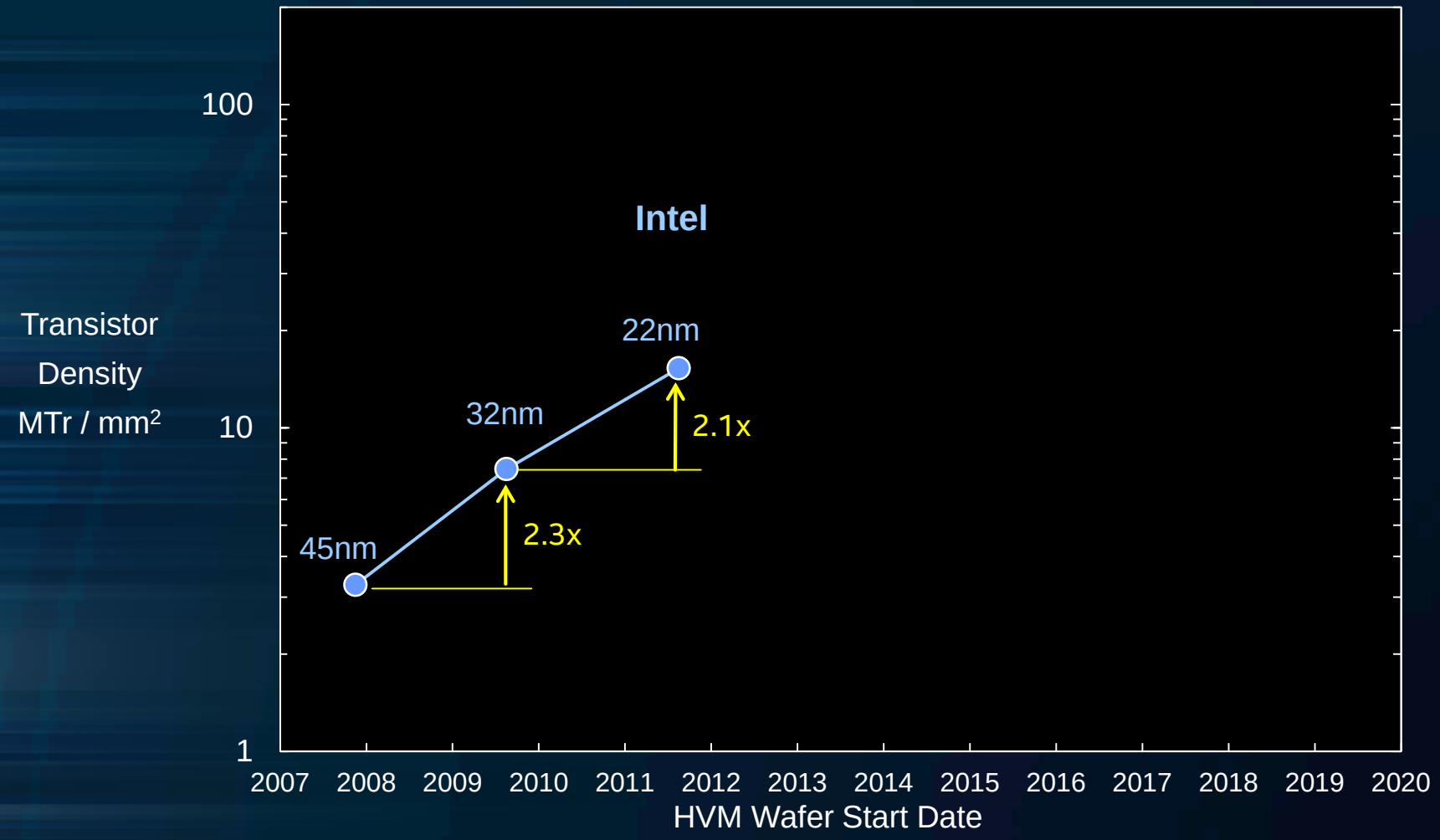


$$0.6 \times \frac{\text{NAND2 Tr Count}}{\text{NAND2 Cell Area}} + 0.4 \times \frac{\text{Scan Flip Flop Tr Count}}{\text{Scan Flip Flop Cell Area}} = \#\ \text{Transistors} / \text{mm}^2$$

Standard NAND+SFF metric is a more accurate estimate of logic transistor density

Source: Intel

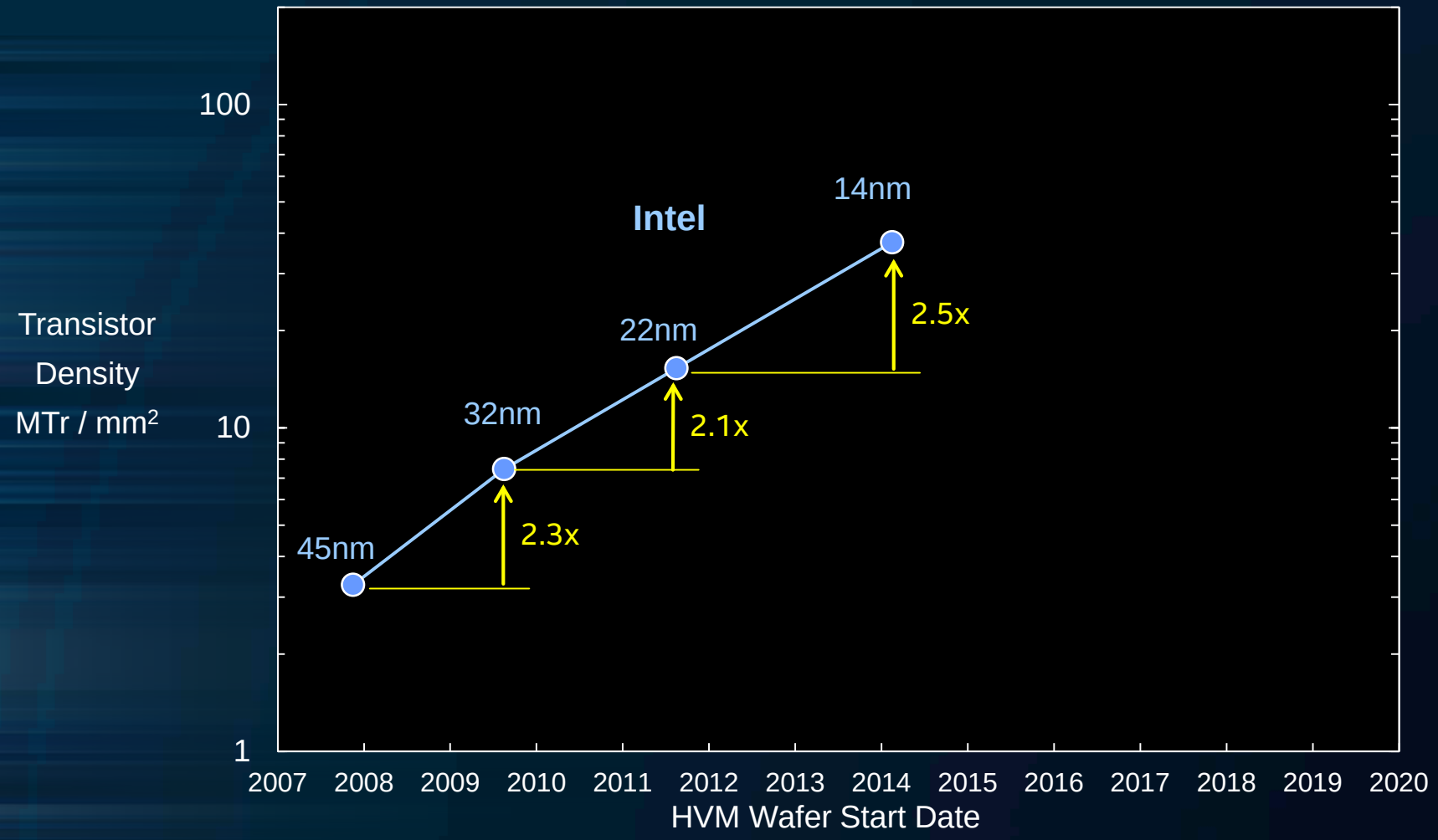
LOGIC TRANSISTOR DENSITY



Logic transistor density improvement was ~2.2x per generation using NAND+SFF metric

Source: Intel

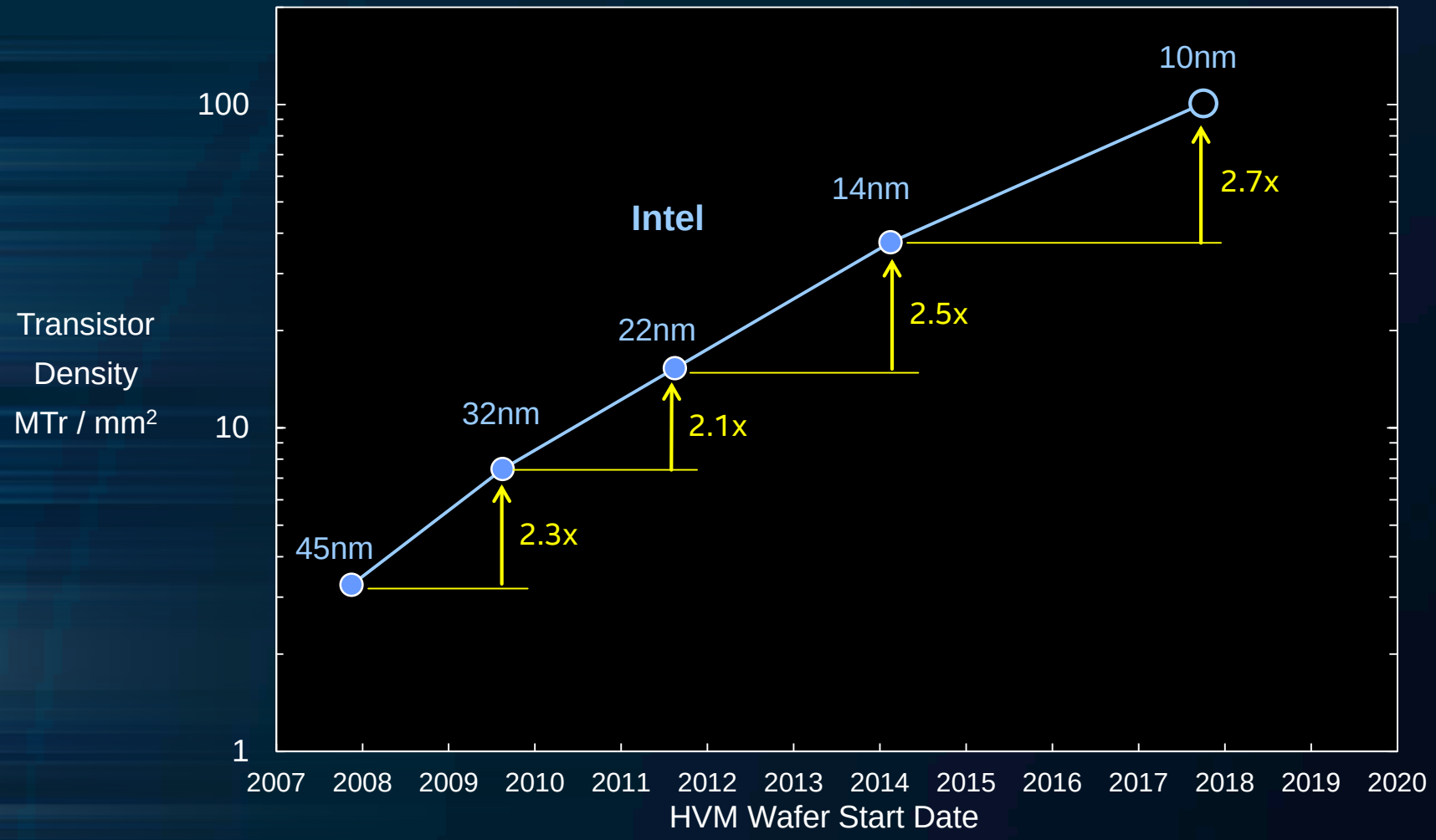
LOGIC TRANSISTOR DENSITY



14 nm hyper scaling provided ~2.5x transistor density improvement

Source: Intel

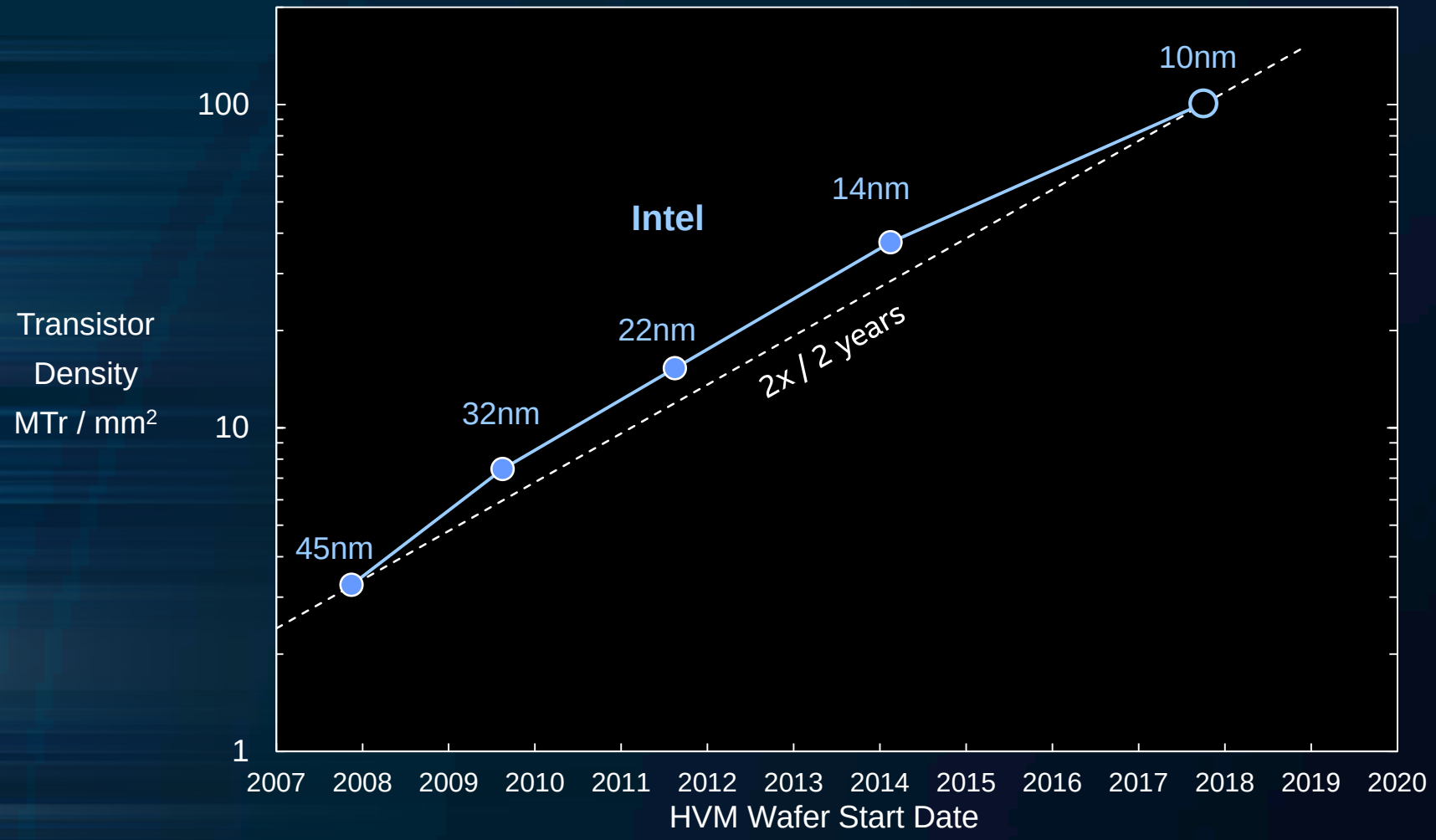
LOGIC TRANSISTOR DENSITY



10 nm hyper scaling provides ~2.7x transistor density improvement

Source: Intel. 2017-2020 are estimates based upon current expectations and available information.

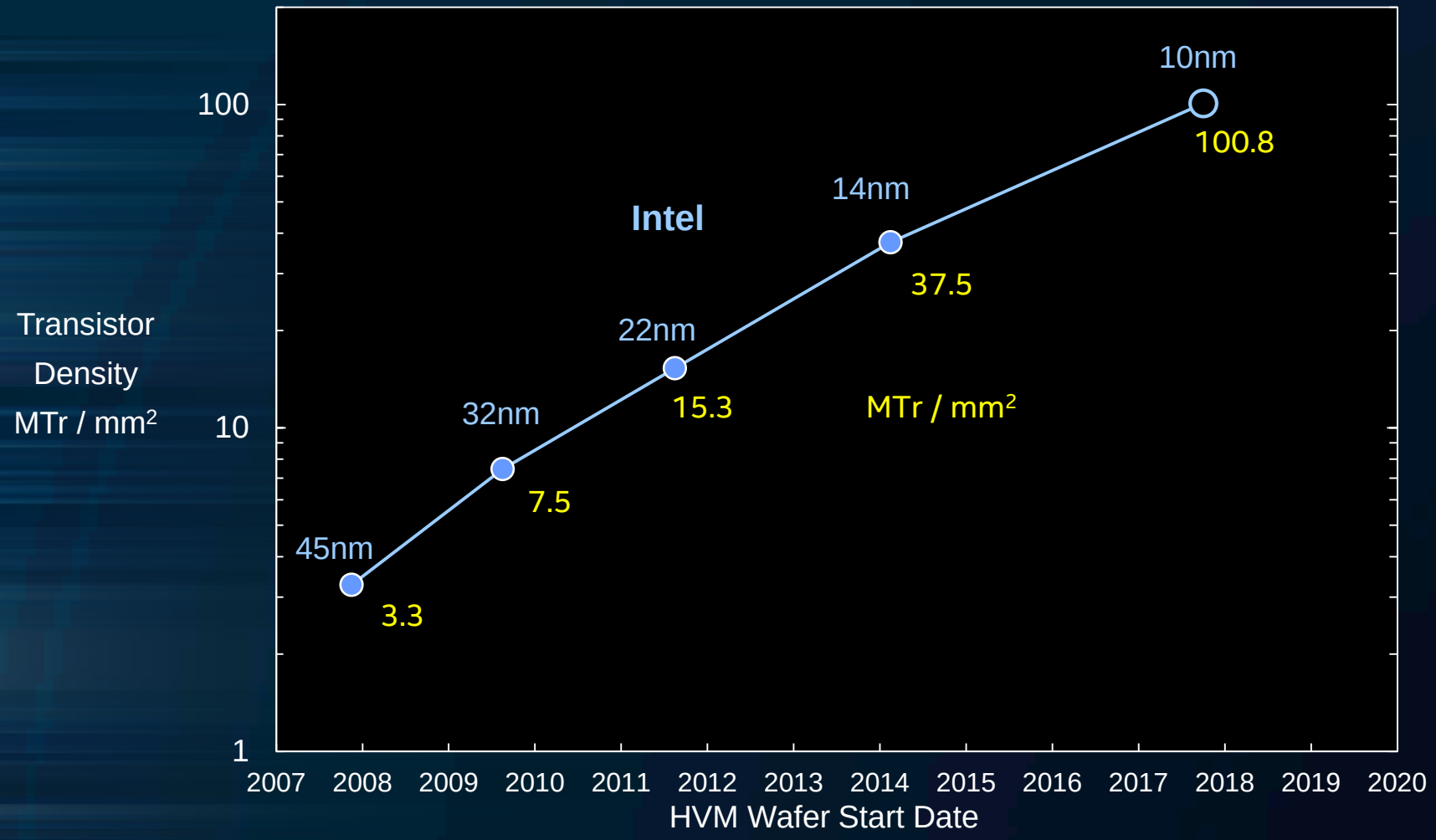
LOGIC TRANSISTOR DENSITY



Transistor density improvements continue at a rate of ~doubling every 2 years

Source: Intel. 2017-2020 are estimates based upon current expectations and available information.

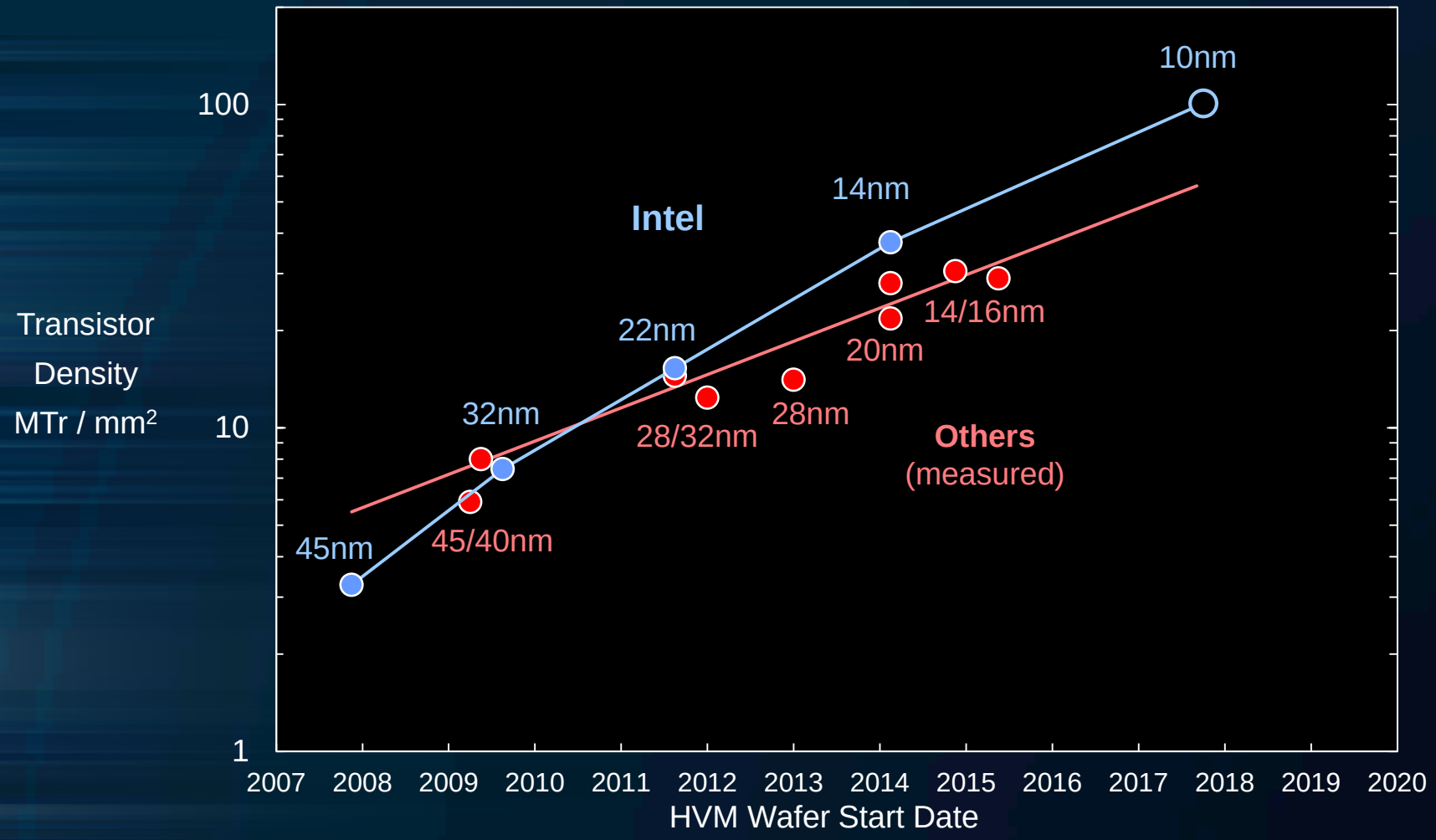
LOGIC TRANSISTOR DENSITY



Logic node names should be accompanied with logic transistor density

Source: Intel. 2017-2020 are estimates based upon current expectations and available information.

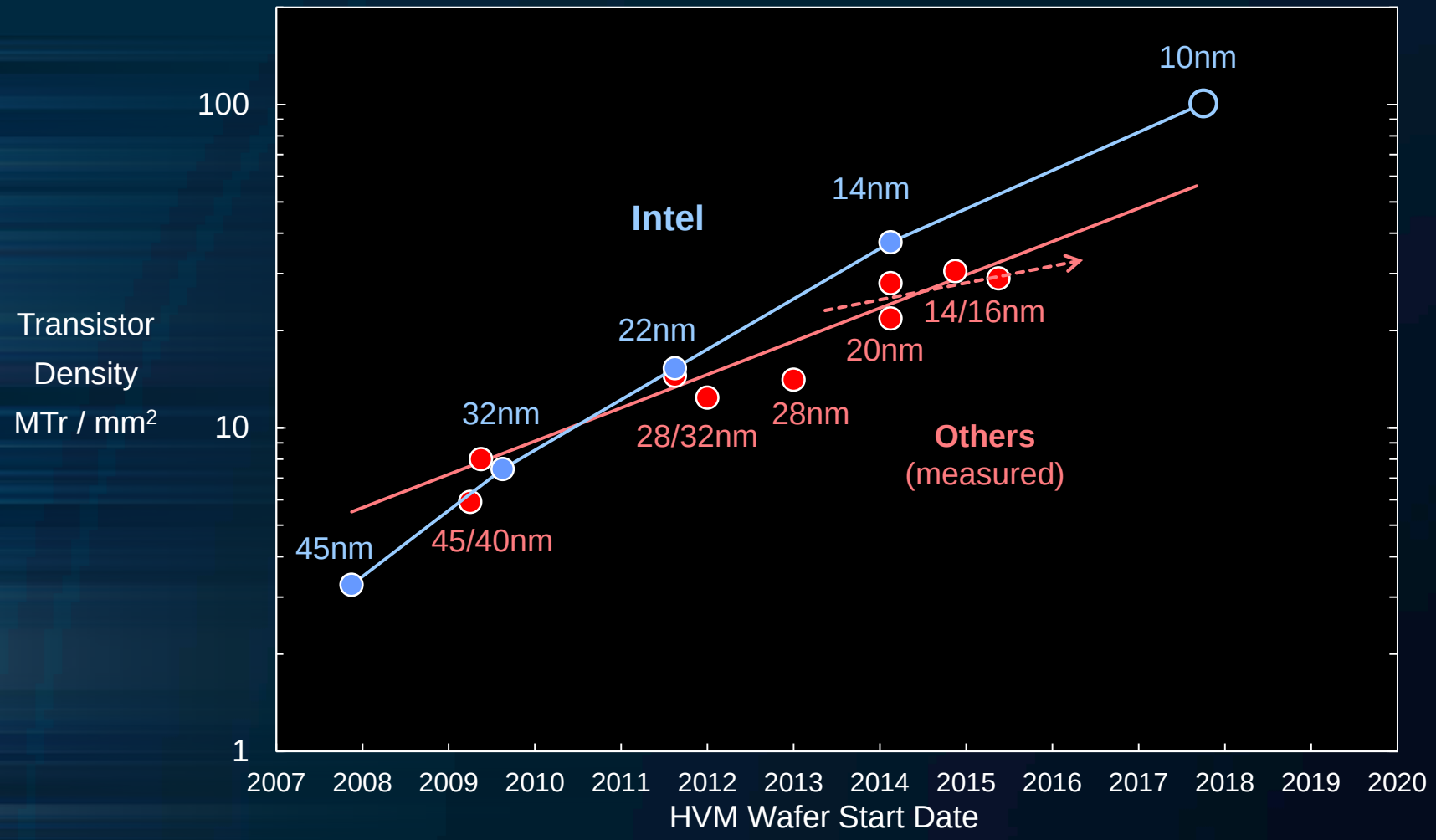
LOGIC TRANSISTOR DENSITY



Other measured transistor densities using same NAND+SFF metric

Source: Amalgamation of analyst data and Intel analysis. 2017-2020 are estimates based upon current expectations and available information.

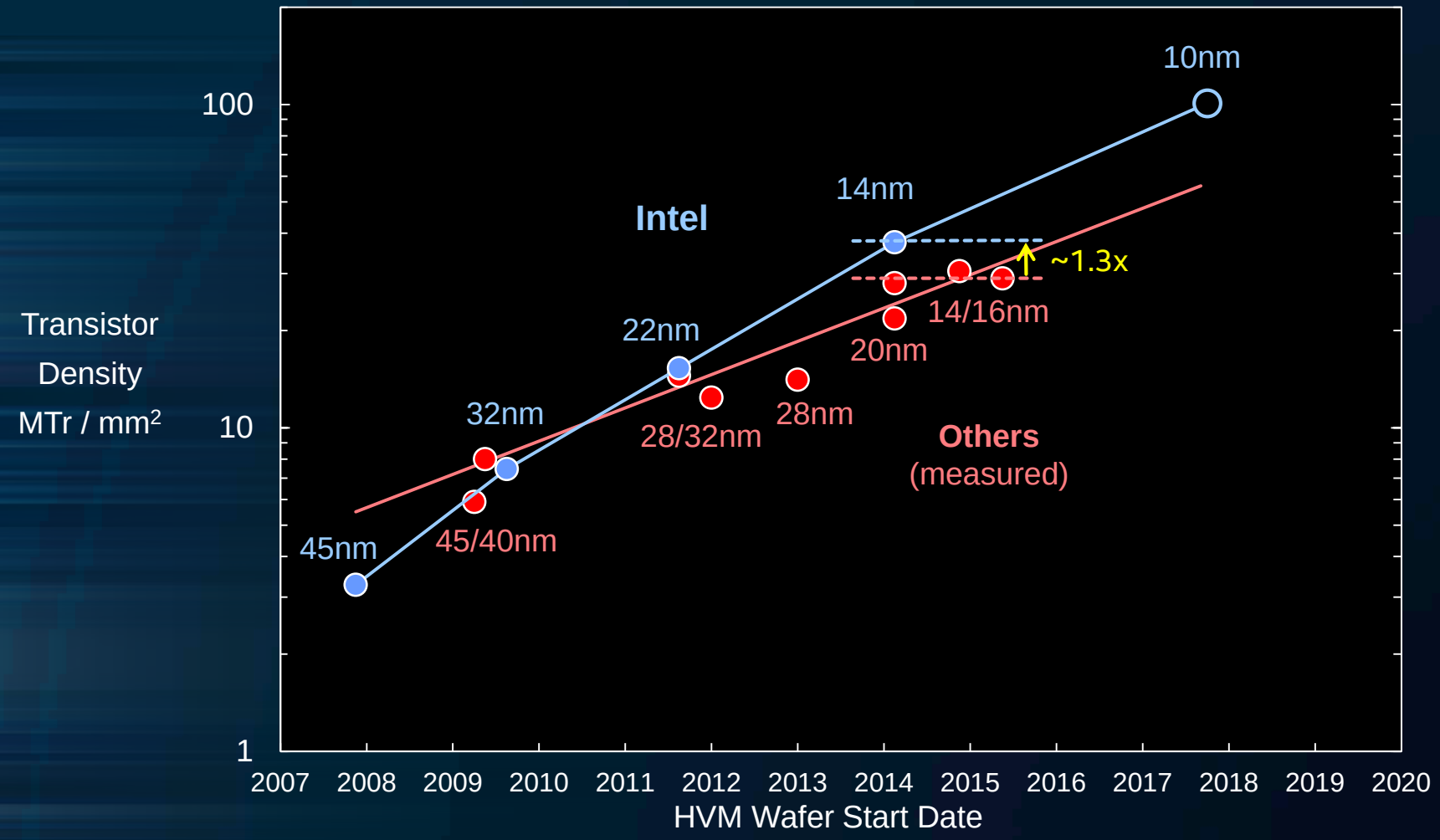
LOGIC TRANSISTOR DENSITY



Rate of density improvement was slow on other 20/16/14 nm technologies

Source: Amalgamation of analyst data and Intel analysis. 2017-2020 are estimates based upon current expectations and available information.

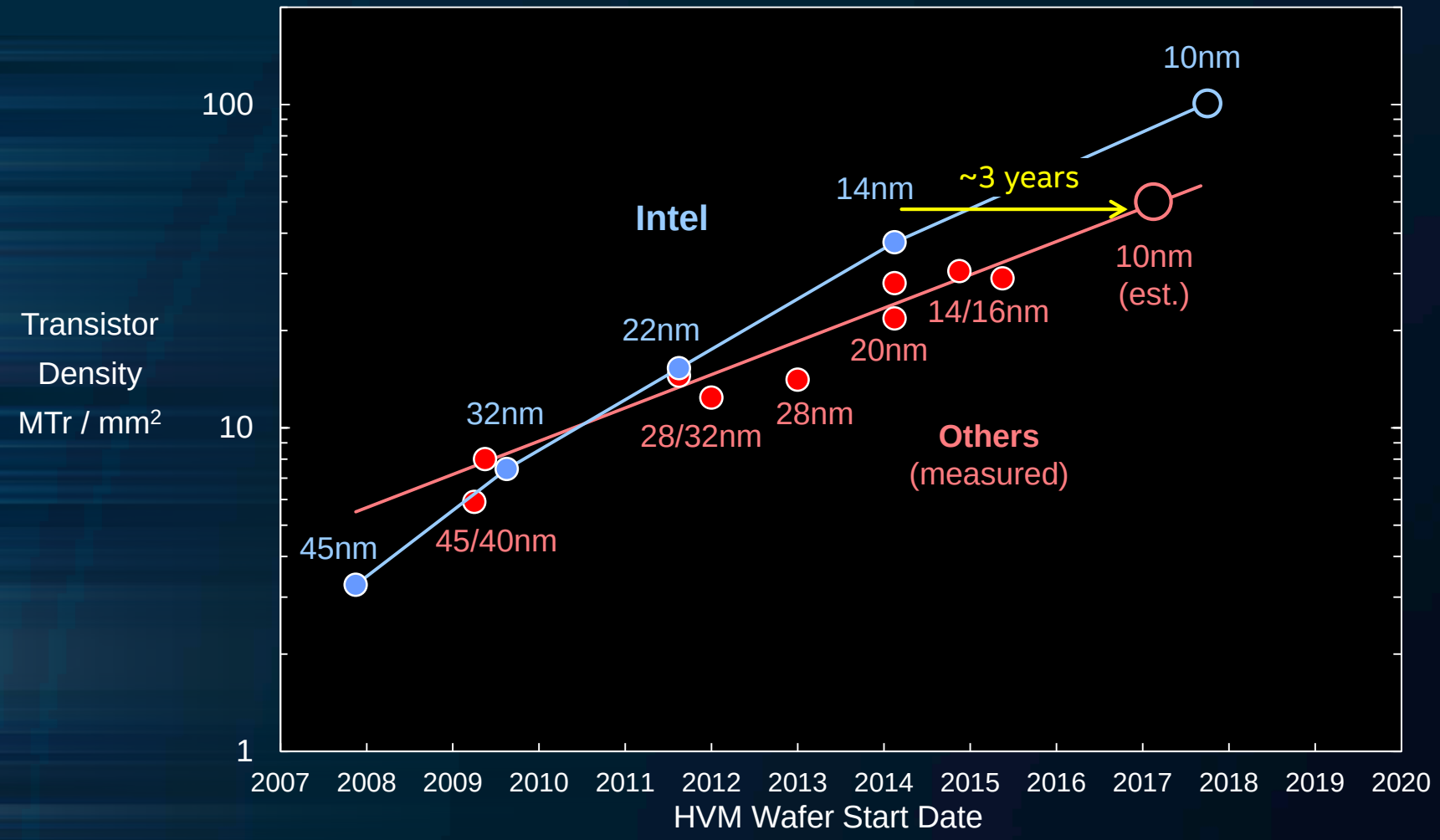
LOGIC TRANSISTOR DENSITY



Intel 14 nm has ~1.3x higher transistor density than other 20/16/14 nm

Source: Amalgamation of analyst data and Intel analysis. 2017-2020 are estimates based upon current expectations and available information.

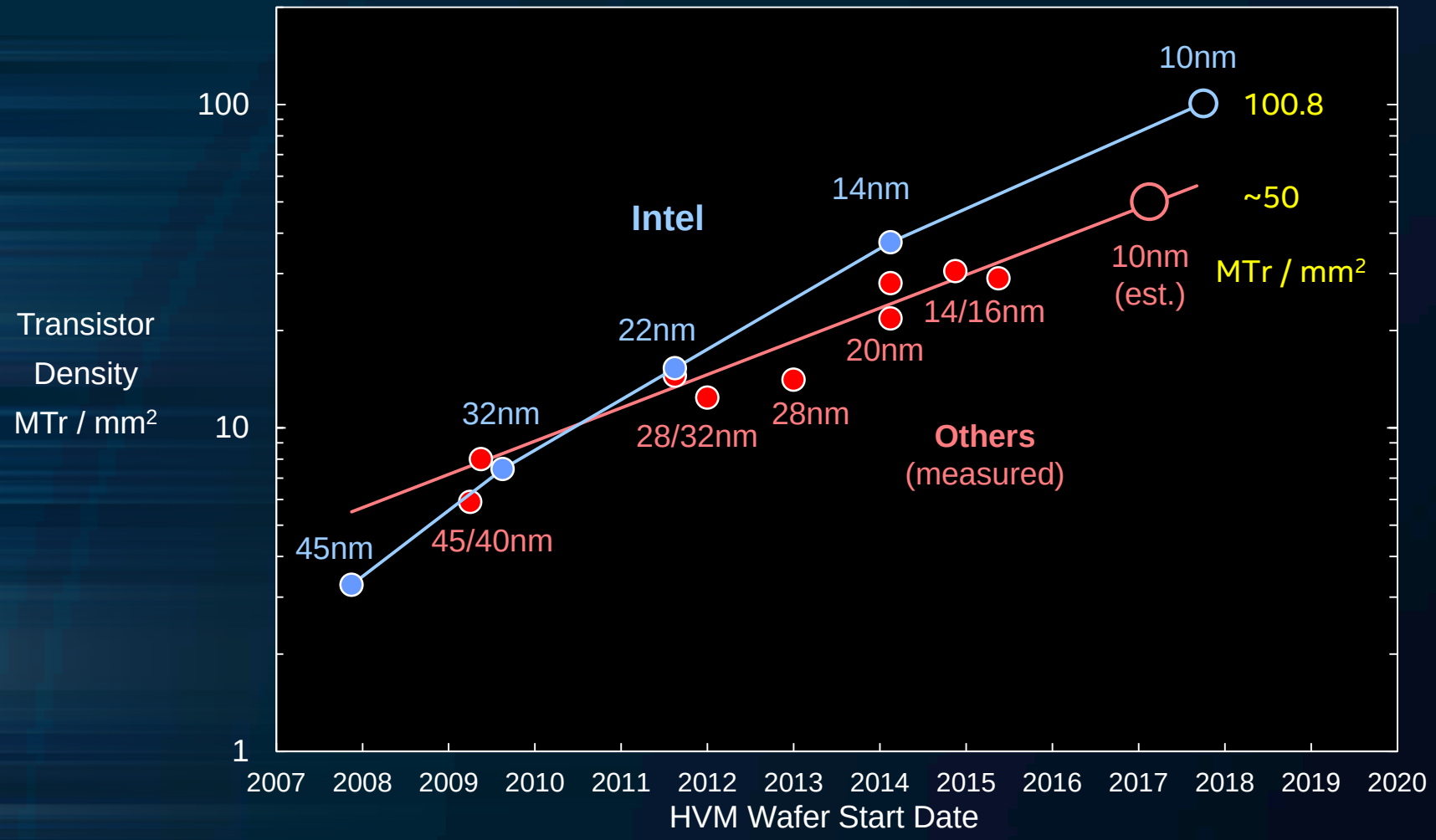
LOGIC TRANSISTOR DENSITY



Other "10 nm" technologies will have density similar to Intel 14 nm, but ~3 years later

Source: Amalgamation of analyst data and Intel analysis. 2017-2020 are estimates based upon current expectations and available information.

LOGIC TRANSISTOR DENSITY



Logic node names should be accompanied with logic transistor density

Source: Amalgamation of analyst data and Intel analysis. 2017-2020 are estimates based upon current expectations and available information.

MOORE'S LAW IS A LAW OF ECONOMICS

LOWER COST

Same circuitry in half the space (Feature Neutral)

OR

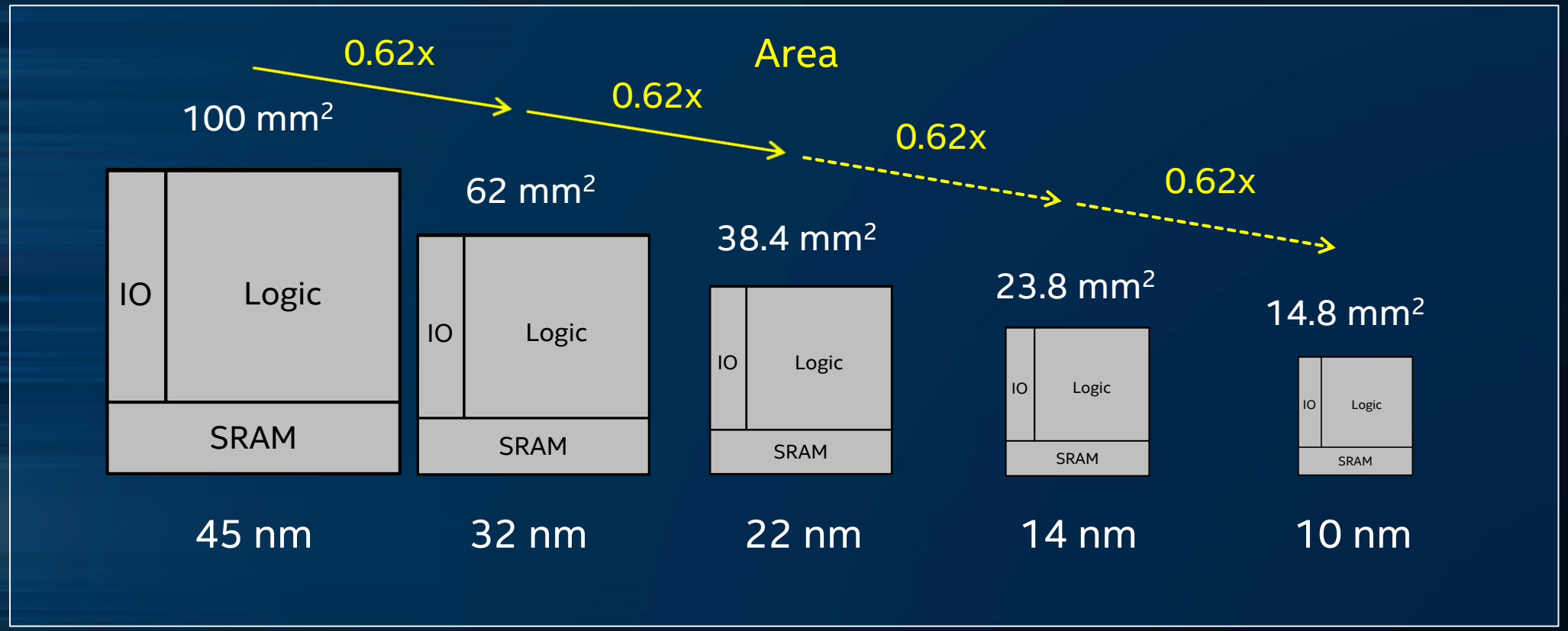
MORE FUNCTIONALITY (more transistors)

Twice the number of transistors in same space

MOORE COST $AVINGS

MOORE PERFORMANCE

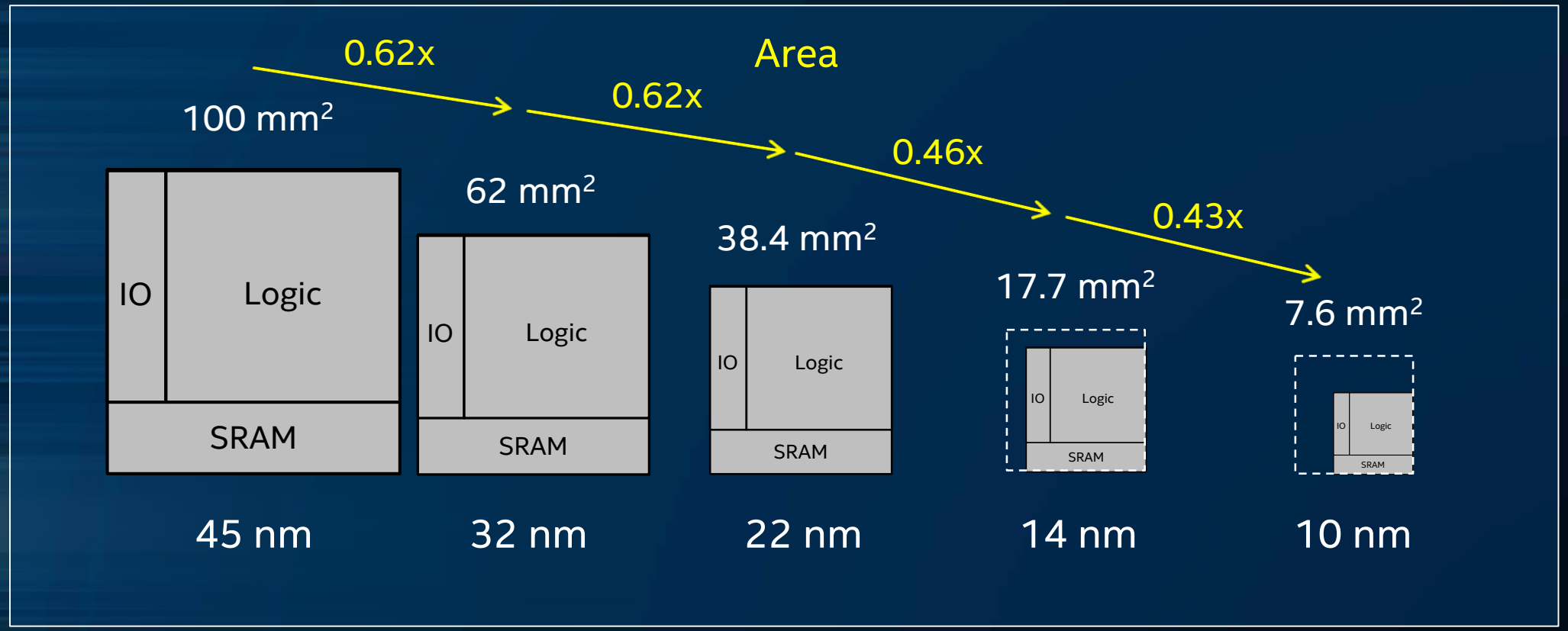
MICROPROCESSOR DIE AREA SCALING



Normal microprocessor die area scaling has been ~0.62x per generation

Source: Intel.

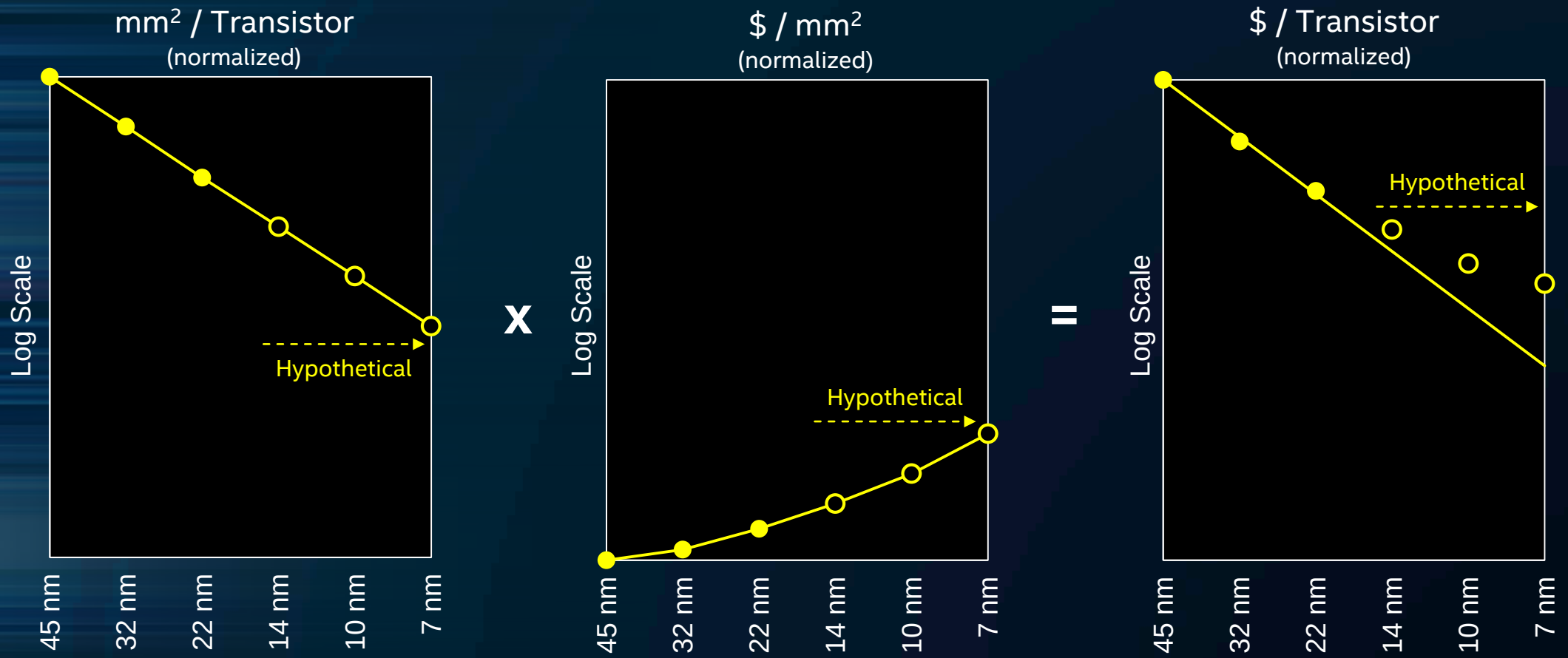
MICROPROCESSOR DIE AREA SCALING



Hyper scaling delivers 0.46-0.43x die area scaling on 14 nm and 10 nm

Source: Intel.

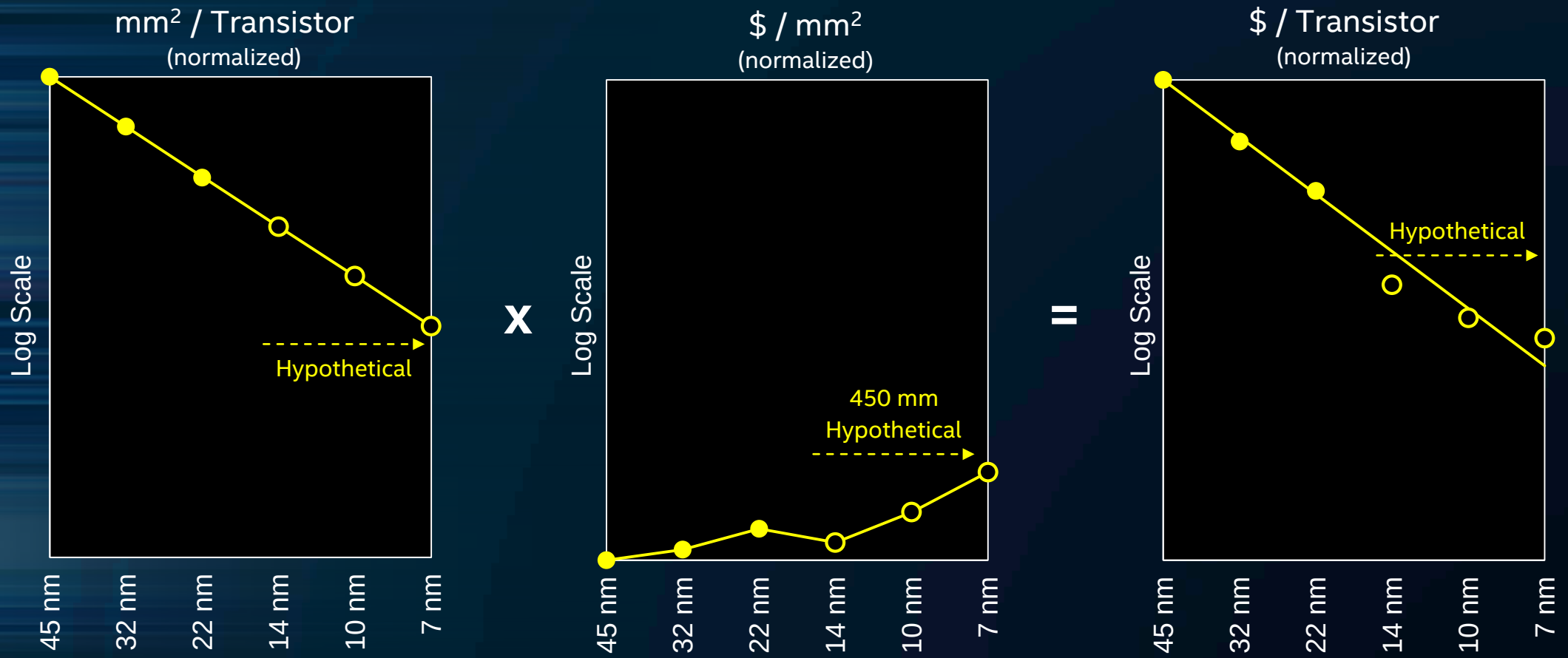
COST PER TRANSISTOR



Normal scaling would have provided poor CPT improvements

Source: Intel.

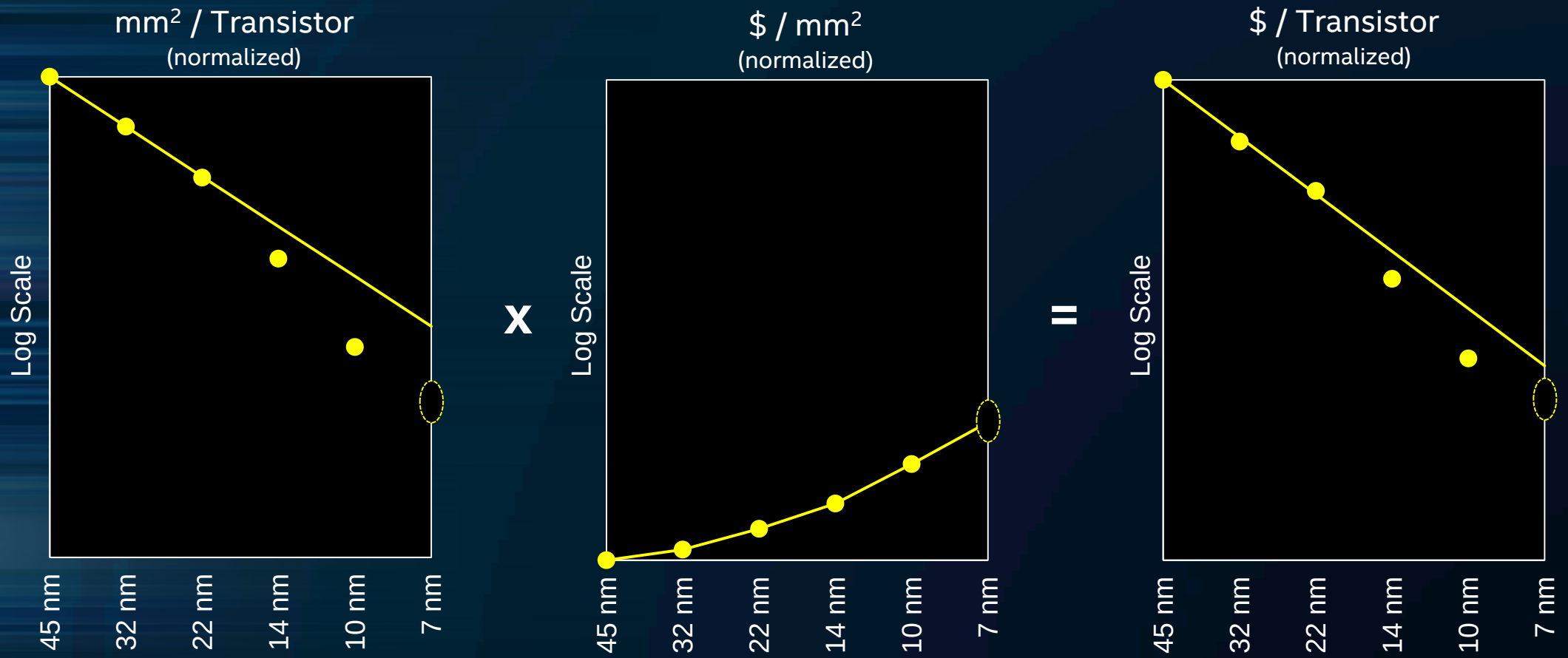
COST PER TRANSISTOR



Normal scaling + 450 mm wafers would have provided better CPT

Source: Intel.

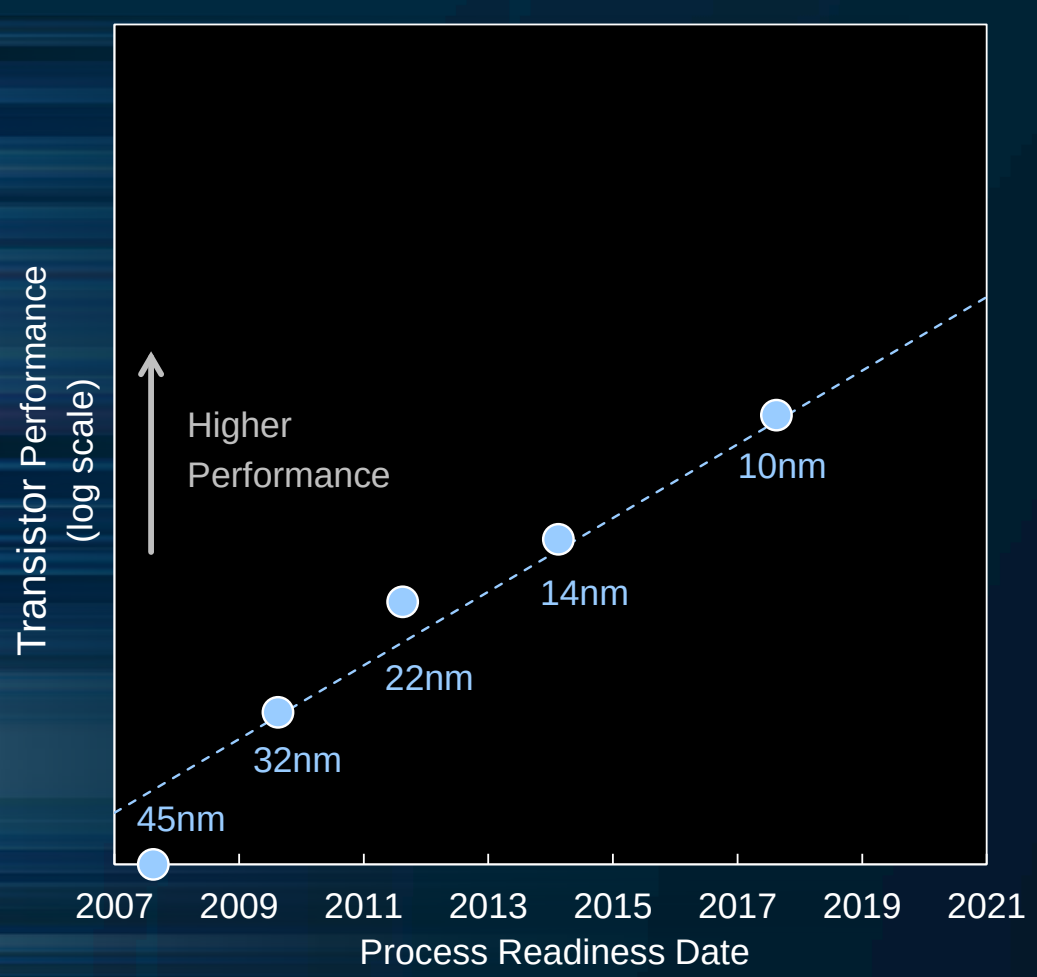
COST PER TRANSISTOR

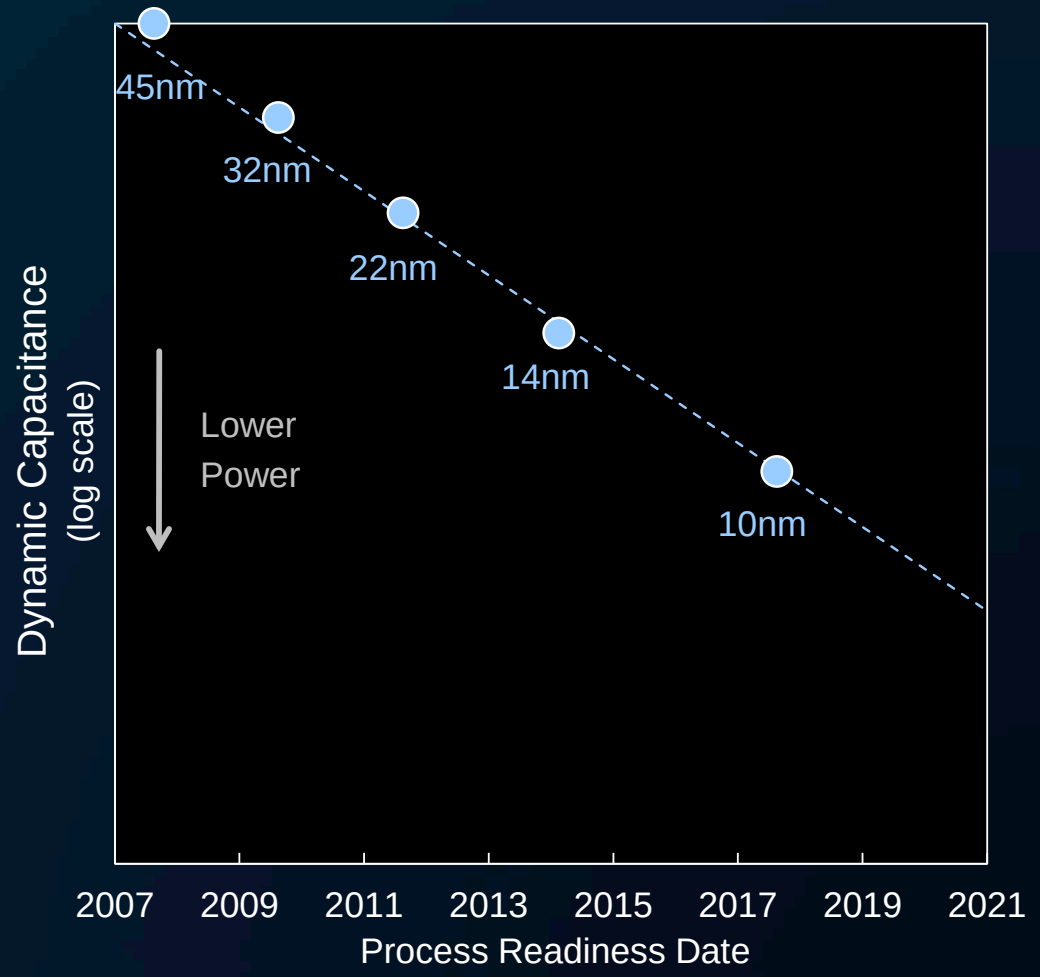


Hyper scaling on Intel 14 nm and 10 nm provides lower CPT

Source: Intel.

TRANSISTOR PERFORMANCE AND POWER

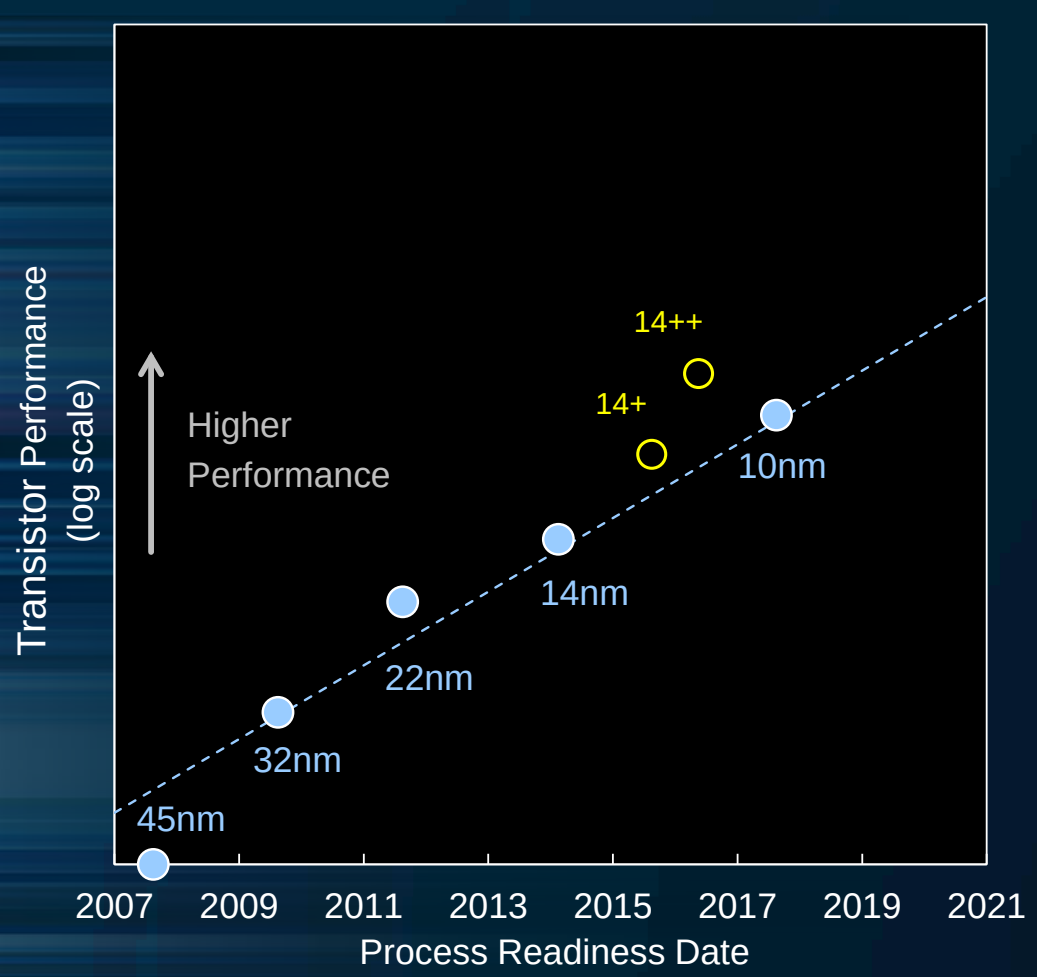


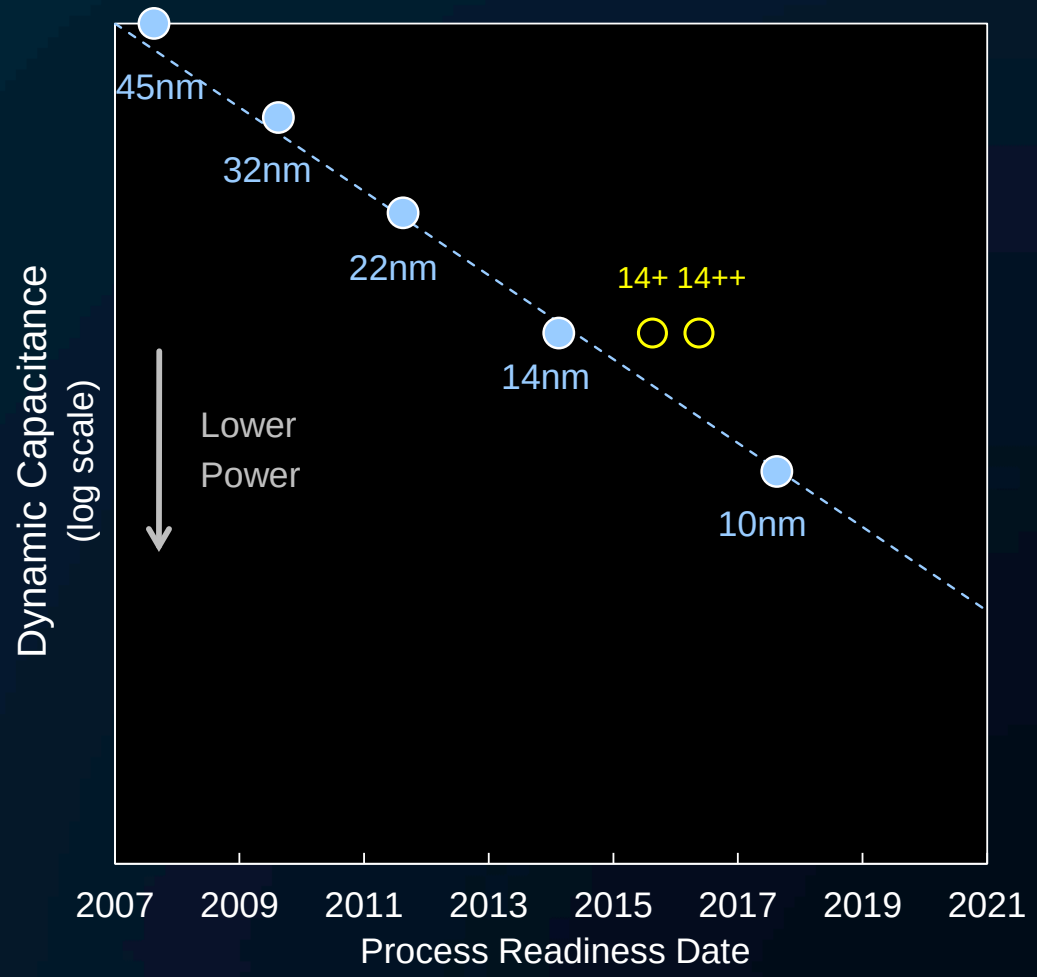


Scaled transistors continue to provide improved performance and lower power

Source: Intel. 2017-2020 are estimates based upon current expectations and available information.

TECHNOLOGY ENHANCEMENTS

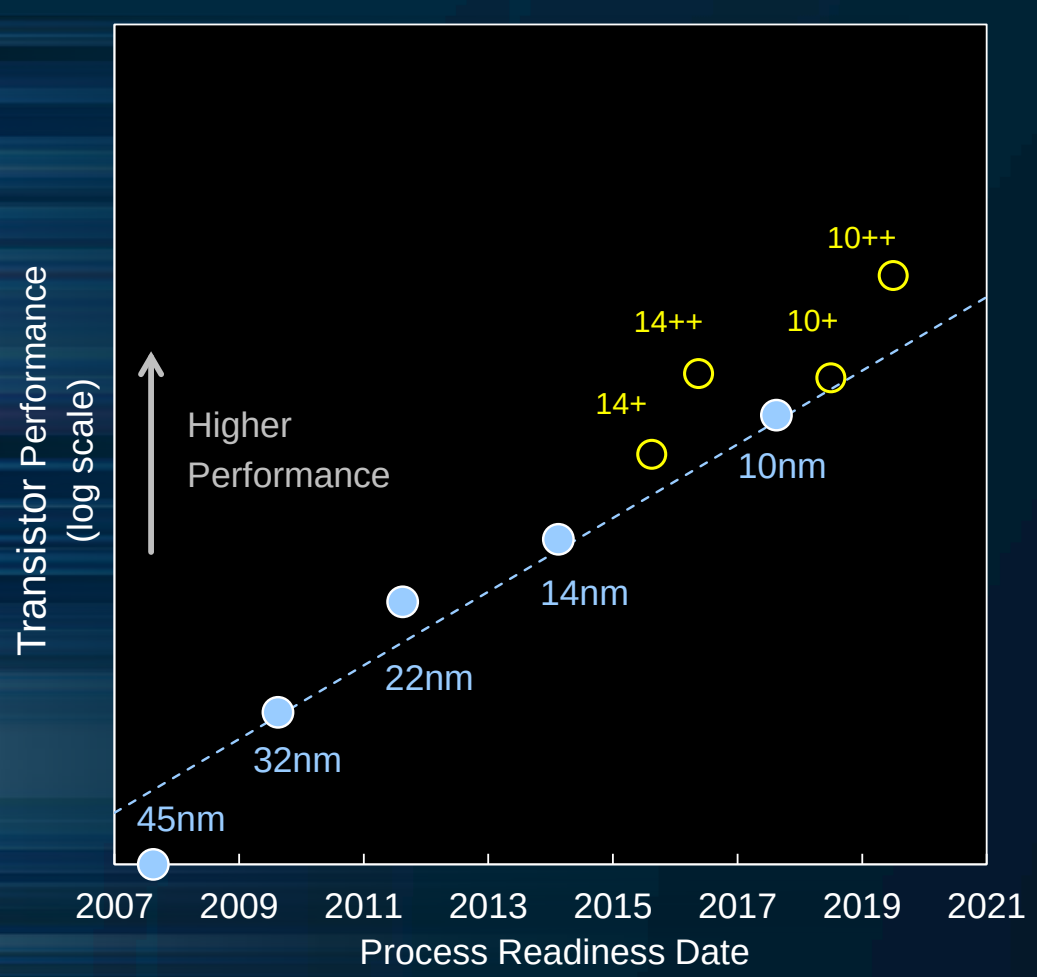


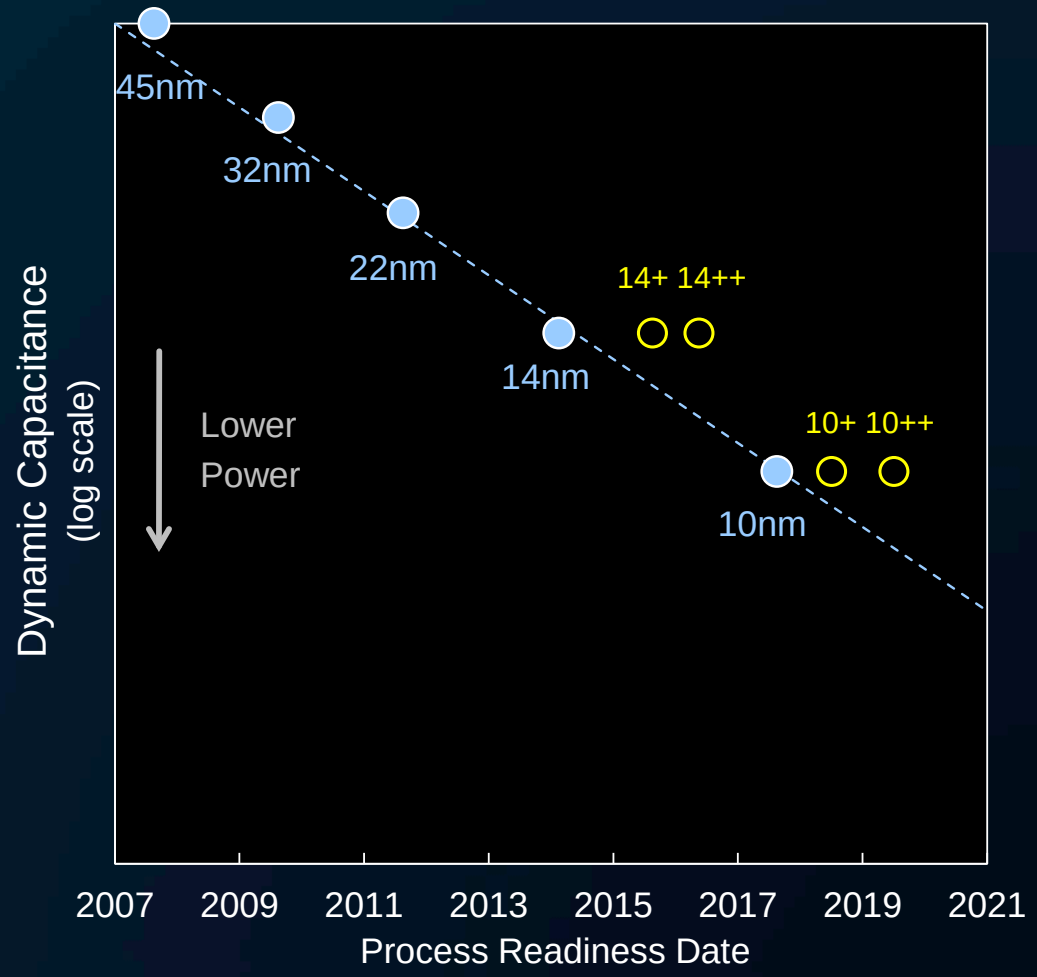


14 nm enhancements improve performance and extend technology life

Source: Intel. 2017-2020 are estimates based upon current expectations and available information.

TECHNOLOGY ENHANCEMENTS





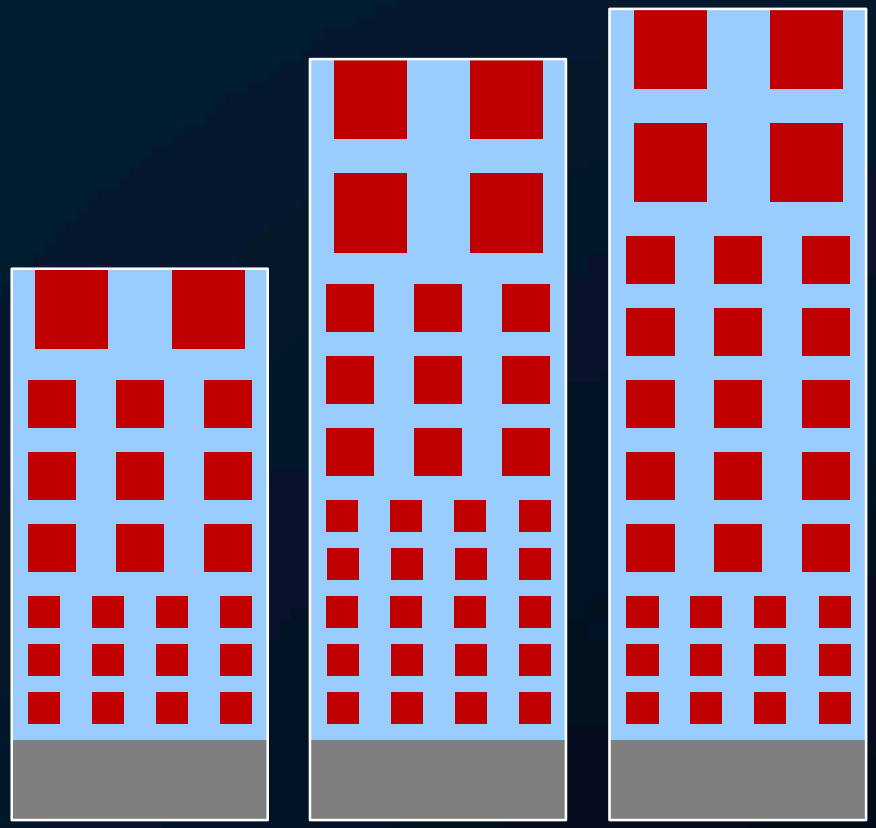
10 nm enhancements improve performance and extend technology life

Source: Intel. 2017-2020 are estimates based upon current expectations and available information.

DERIVATIVE TECHNOLOGIES

	CPU	SoC
High Perf Transistors	Yes	Yes
Low Leakage Transistors	-	Yes
Analog/RF Transistors	-	Yes
HV I/O Transistors	-	Yes
High-Q Inductors	-	Yes
Precision Resistors	Yes	Yes
MIMCAP	Yes	Yes

Device Options

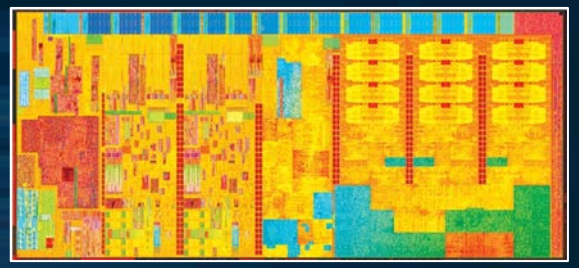


Interconnect Stack Options

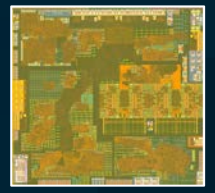
Multiple derivative options offered for each technology generation

Source: Intel

14 NM PRODUCTS

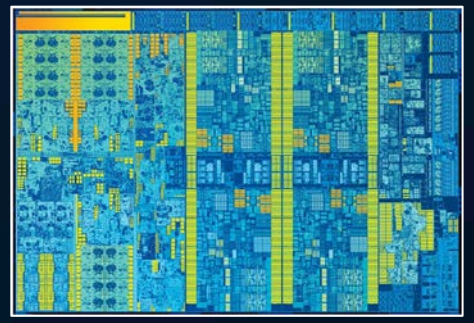


Client



Mobile

Mobile



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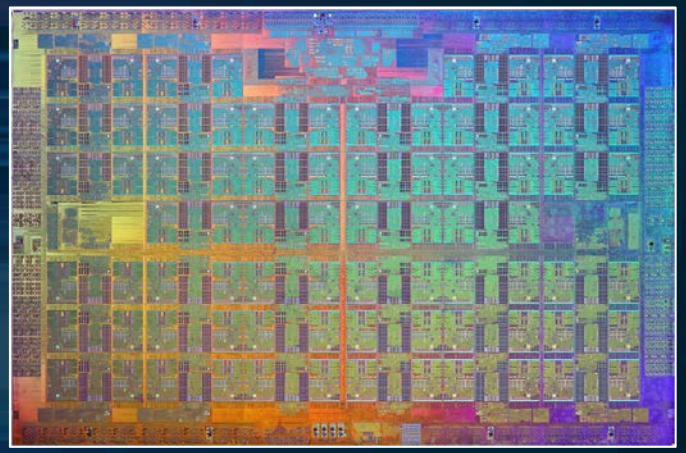

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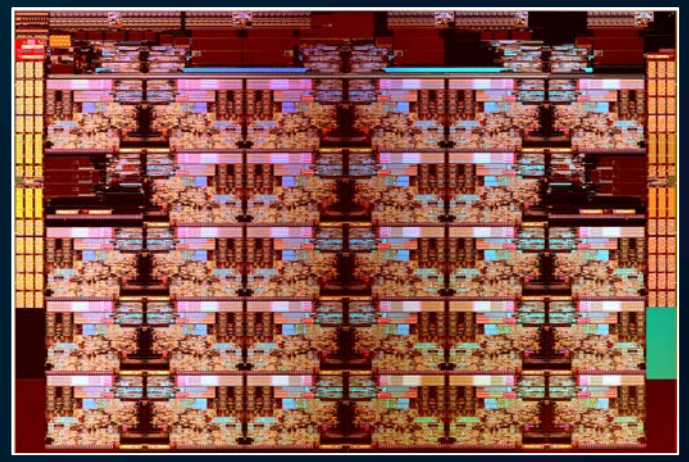

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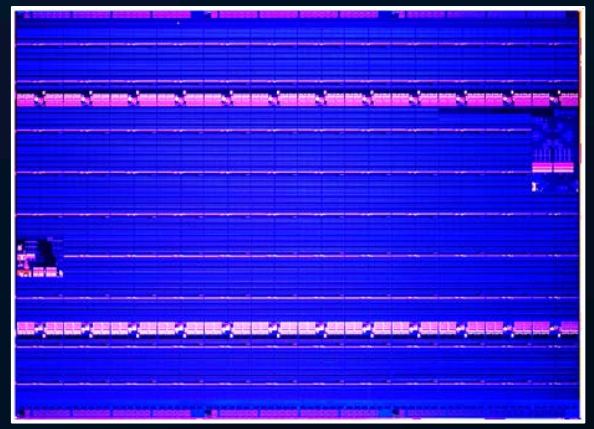
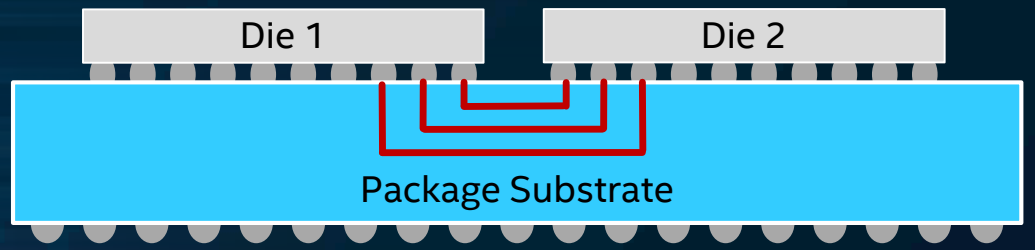


FPGA

Wide range of 14 nm products in volume production on various derivative technologies

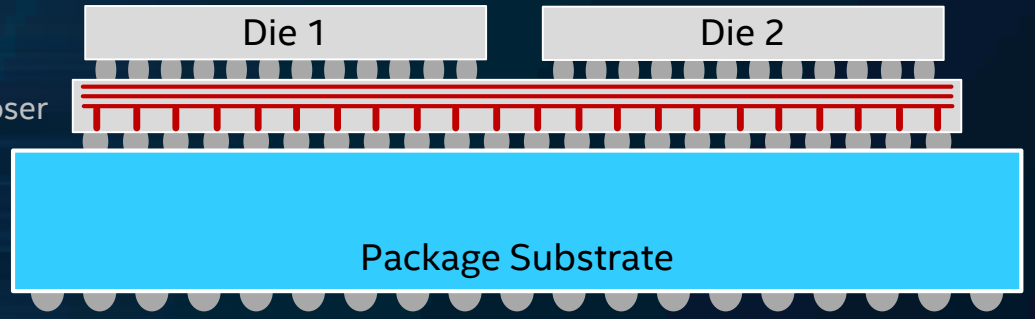
HETEROGENEOUS INTEGRATION OPTIONS

Multi-Chip Package



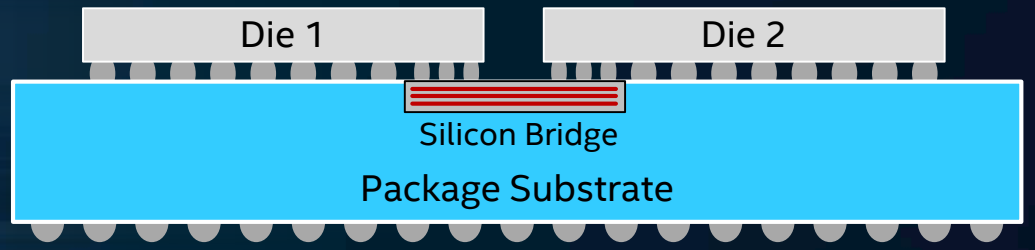
- Poor density of die-package connections
- Poor density of die-die interconnects

Silicon Interposer



- Good density of die-interposer connections
- Good density of die-die interconnects
- Higher cost of large interposer + thru-silicon vias

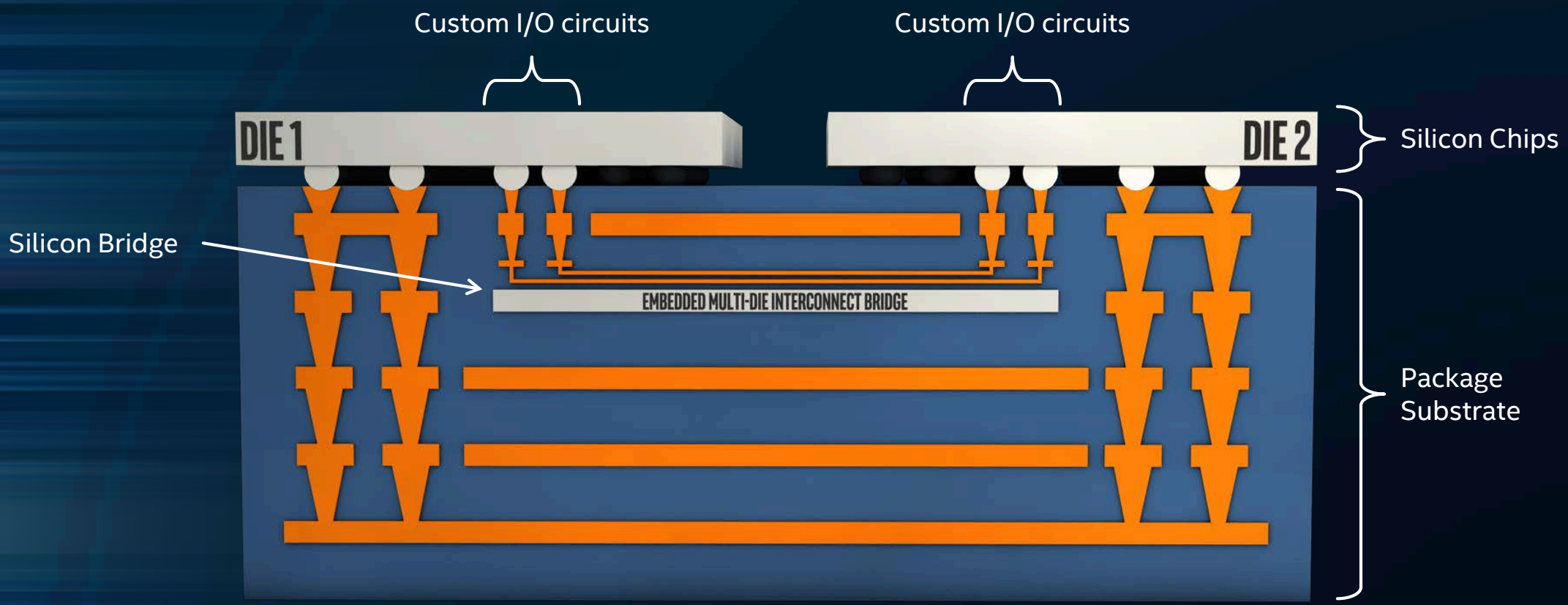
Embedded Multi-Die Interconnect Bridge



- Good density of die-bridge connections
- Good density of die-die interconnects
- Low cost of small silicon bridges

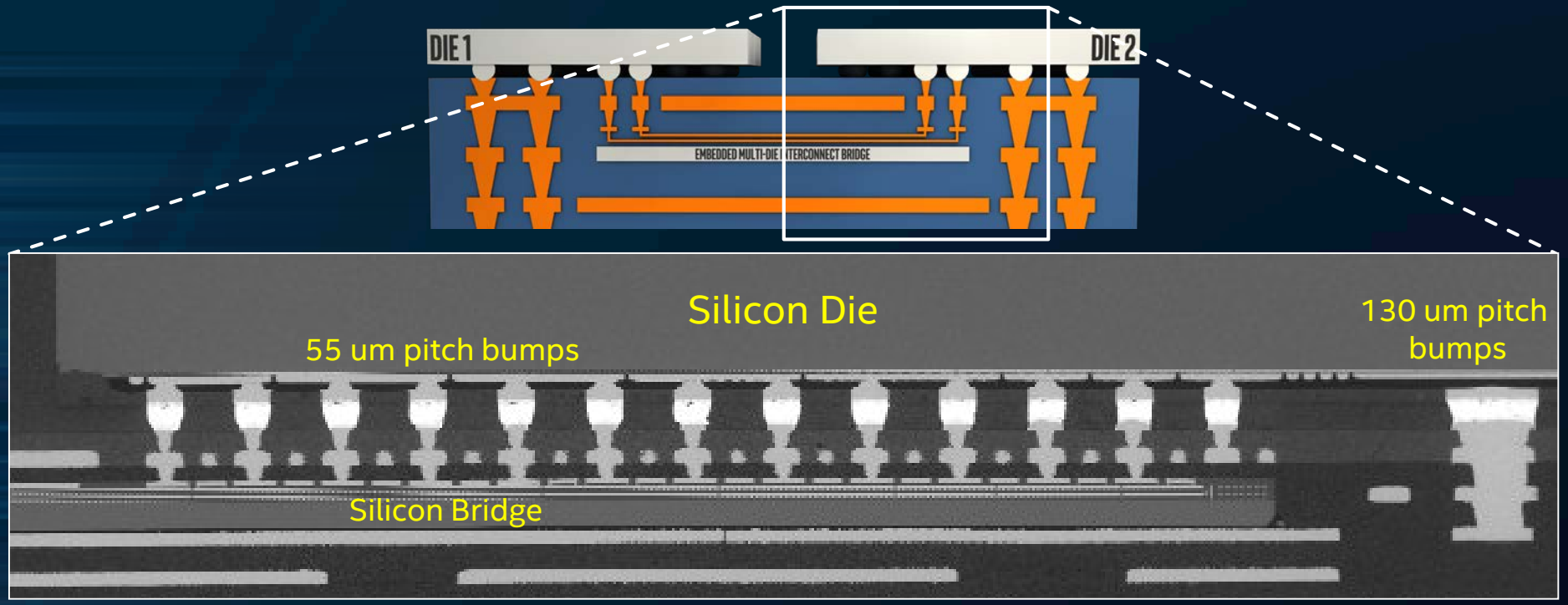
EMIB technology provides high density, high bandwidth die-die interconnects

EMBEDDED MULTI-DIE INTERCONNECT BRIDGE

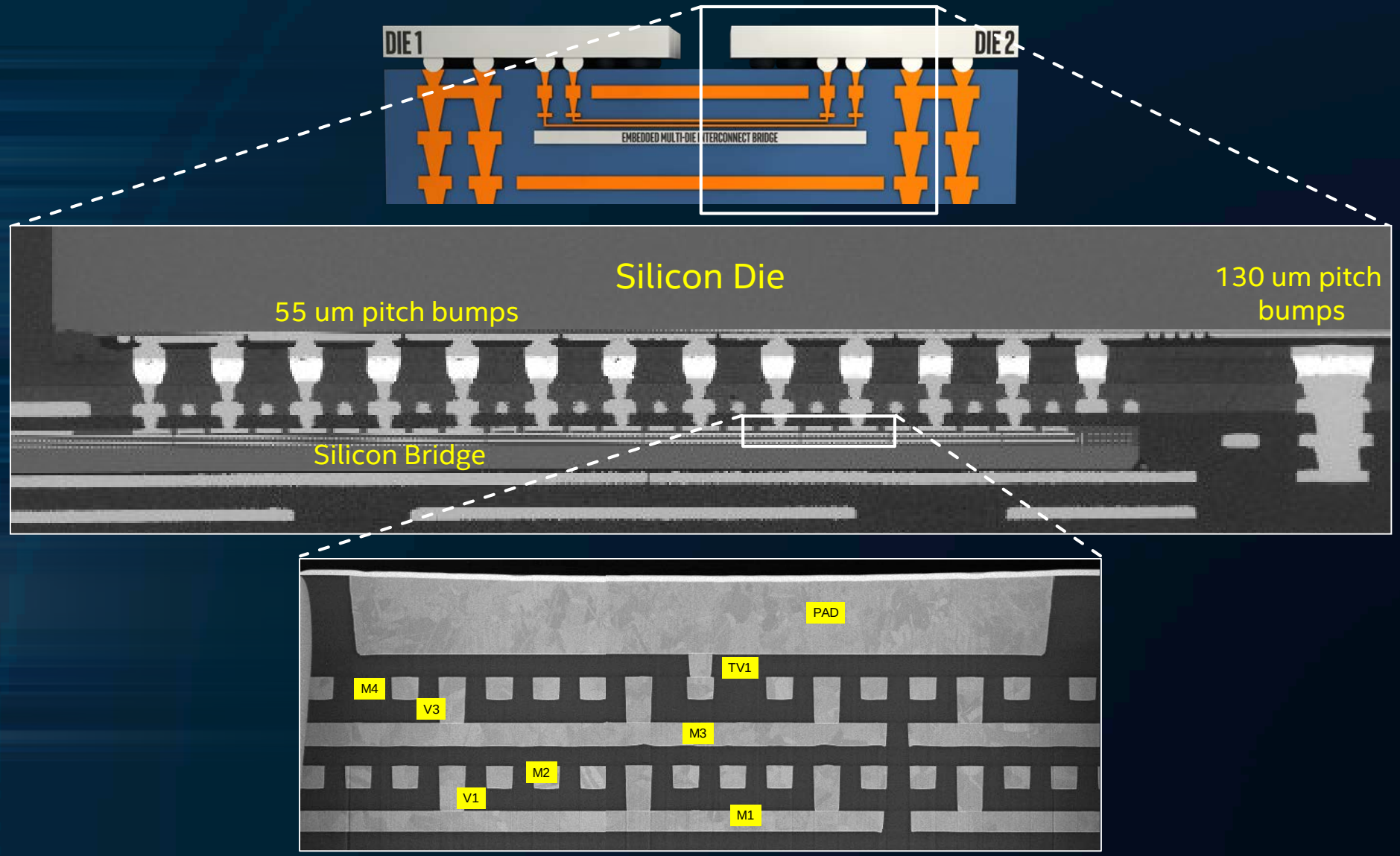


EMIB technology provides high density, high bandwidth die-die interconnects

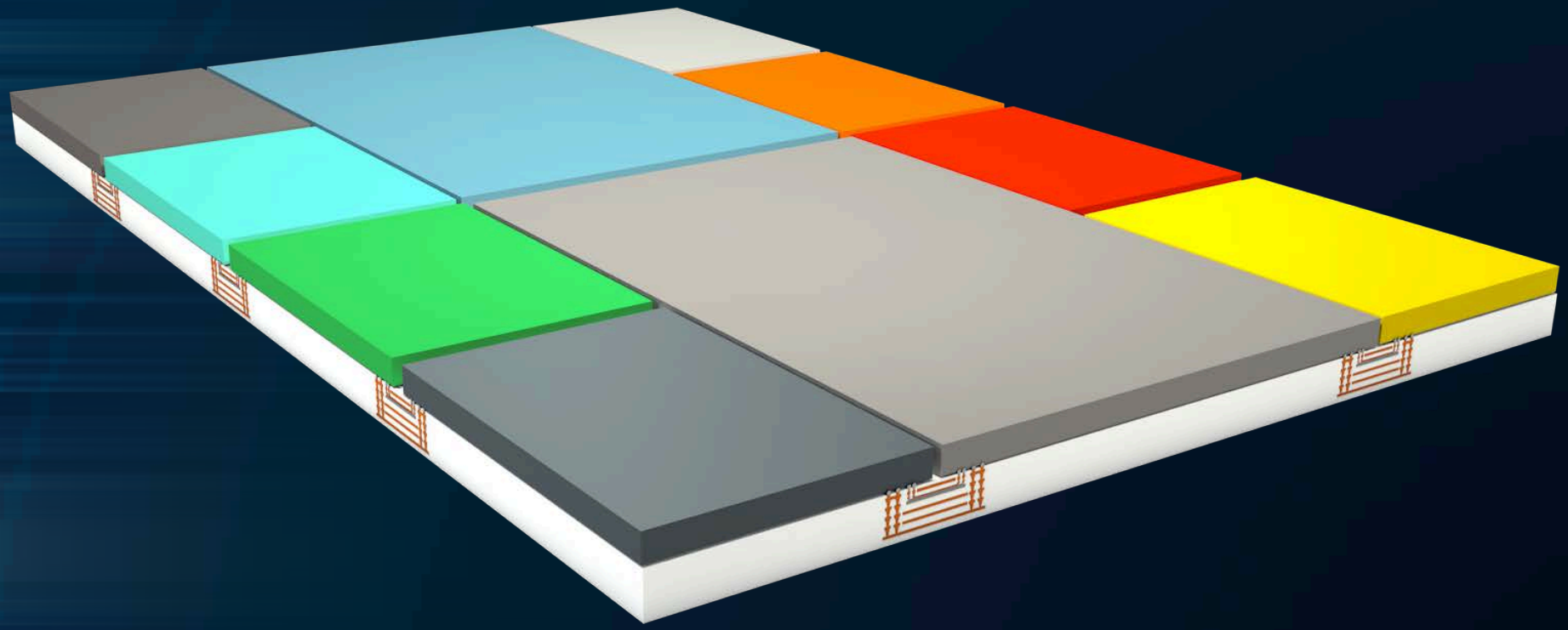
EMBEDDED MULTI-DIE INTERCONNECT BRIDGE



EMBEDDED MULTI-DIE INTERCONNECT BRIDGE



HETEROGENEOUS INTEGRATION



EMIB enables dense and cost effective in-package heterogeneous integration

KEY MESSAGES

- Intel leads the industry in introducing innovations that enable scaling
- Hyper scaling on Intel 14 nm and 10 nm provides better-than-normal scaling while continuing to reduce cost per transistor
- Intel's 14 nm technology has ~3 year lead over other "10 nm" technologies with similar logic transistor density
- Intel's 10 nm technology provides industry-leading logic transistor density using a quantitative density metric
- Enhanced versions of 14 nm and 10 nm provide improved performance and extend the life of these technologies

Moore's Law is alive and well at Intel

Source: Amalgamation of analyst data and Intel analysis, based upon current expectations and available information.

LEADING AT THE EDGE

TECHNOLOGY AND MANUFACTURING DAY