A 7nm CMOS Platform Technology Featuring 4th Generation FinFET Transistors with a 0.027um^2 High Density 6-T SRAM cell for Mobile SoC Applications

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Abstract

For the first time, a leading edge 7nm CMOS platform technology for mobile SoC applications is presented. This technology provides >3.3X routed gate density and 35%~40% speed gain or >65% power reduction over our 16nm FinFET technology. A fully functional 256Mb SRAM test-chip with the smallest high density SRAM cell of 0.027um^2 is demonstrated down to 0.5V. The 4th generation FinFET transistors are optimized with device mismatch reduction by 25%~35% and multi-Vt device options to enable low power and high performance design requirements.

Introduction

The adoption of FinFET transistors with excellent device electrostatic characteristics in our 16nm CMOS technology [1-2] has been successfully proven in volume production for low power and high performance applications. The feasibility of extending scaled bulk FinFET transistors for advanced CMOS technology beyond 10nm node with key process enablers was illustrated [3]. We expect the rise of connected or smart devices in IoT and VR/AR applications, very low power combined with low cost to be the key driver for future technology. It is important to develop the best time-to-market technology solution with sufficient PPAC to capture the business opportunities. This paper presents the state-of-art 7nm CMOS technology integrated with 4th generation FinFETs and up-to-date the smallest high density SRAM cell for low power applications.

Process Architecture

A smart shrink approach combined with critical ground rule scaling is adopted to achieve the desired chip density and die cost reduction. Advanced pitch-splitting patterning technique with 193nm immersion lithography is used to enable pitch scaling for critical layers. Fin width and profile are carefully optimized to maintain excellent short channel effect with scaled gate length to reduce parasitic capacitance between contact and gate. The 5th generation high-K metal gate (HK/MG) RPG process with dual-gate oxide flow is employed to support core and I/O devices for SoC design. Raised source/drain with dual epitaxy process is optimized in order to provide the necessary channel strain and to reduce source/drain (S/D) parasitic resistance. A novel contact process is developed to support tight CPP scaling with robust contact-to-gate isolation. Advanced Cu/low-k interconnect process scheme with different metal pitches and stacks is tailored for metal resistance and capacitance optimization. Minimum metal pitch scaling is enabled using advanced patterning scheme, whereas single patterning is adopted for metal layers with 2X minimum metal pitch and above.

Transistor Performance

This technology offers >40% speed gain or >65% total power reduction over our 16nm technology [1-2] based on Figure of Merits (FOM) consists of Inverter, NAND, and NOR circuitry with a fan-out of 3 (F.O.=3) as shown in Figure 1. Fin width and profile are co-optimized with CET reduction to sustain short channel behavior for Lg scaling. Figure 2, superior electrostatic of core transistors with competitive DIBL of ~40mV/V at smaller effective gate length down to 15nm is illustrated. In addition, typical Id-Vg curves of core devices with sub-threshold swing of ~65mV/decade are shown in Figure 3. Multi-Vt device options with Vt range ~200mV are developed to enable design flexibility for power and performance trade-off as shown in Figure 4. Furthermore, Figure 5 illustrates the use of novel strain engineering and new process knobs to obtain device drive current

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gain by 30% and 40% through mobility boost and parasitic resistance reduction for NMOS and PMOS, respectively.

Device analog characteristics are also enhanced through process optimization. Reduction of device Vt mismatch (AVt) by 25% and 35% for NMOS and PMOS, respectively, is achieved in Figure 6. Thermal noise of the FinFET devices in this work is improved through gate resistance reduction as shown in Figure 7. Critical analog FOMs including Operational Trans-conductance Amplifier (OTA) and Band-Gap Reference circuit (BGR) are characterized to quantify the benefits of device optimization for analog design. In Figure 8, substantial improvement in OTA gain can be obtained via device LDD junction profile tuning. Bipolar mismatch reduction improves BGR accuracy is achieved with fin profile optimization as illustrated in Figure 9.

SRAM and Interconnect

Competitive HD and HC SRAM cells are offered for low leakage, high performance and low Vccmin applications. Figure 10 compares SRAM array density and speed gain of this work with those reported in [1-2]. The 7nm technology reported in this paper provides >2.6X SRAM array density with >80% array speed gain over our 16nm technology at the same voltage. The butterfly curves of the 0.027um^2 HD SRAM cell measured at different voltages are shown in Figure 11, where the excellent cell stability down to 0.45V is clearly demonstrated. The static noise margin (SNM) of 102mV and 70mV are achieved for 0.6V and 0.45V operation, respectively. A yield learning vehicle consists of SRAM test-chips for both HD and HC 6-T SRAM cells is used for technology development. The Shmoo plot of a 0.027um^2 high density 256Mb SRAM macro illustrates full read and write capability down to 0.5V as shown in Figure 12. To our knowledge, this is the smallest fully functional SRAM cell ever reported [3-4].

Advanced pitch-splitting patterning is adopted to realize the minimum metal pitch of 40nm. Process robustness is characterized by examining metal resistance of line A vs. line B for M0 and Mx layers. As shown in Figure 13, comparable metal resistance and distribution between line A and line B is achieved. Fig.14a shows a cross-section view of 12-level Cu/low-k metal stacks consist of 1X pitch metal (M0 to M4), 1.9X pitch metal (M5 to M9), 3.1X pitch metal (M10) and 18X pitch metal (M11-M12). The Rc distribution of stacked contact to via chain for 4-level and 12-level metals is shown in Fig. 14b with good yield and tight control.

Device and Interconnect Reliability

Key device reliability of the 4th generation FinFETs like time-dependent-dielectric-breakdown (TDDB), bias-temperature-instabilities (BTI) and hot carrier injection (HCI) are examined and characterized. In Figure 15, comparable NMOS TDDB and PMOS NBTI lifetimes with those of our 16nm technology [1-2] can be achieved with careful post high-k/MG thermal optimization. In addition, I/O devices are also optimized by junction doping profile to reduce S/D to substrate leakage current and hence enhance hot carrier immunity as shown in Figure 16.

Interconnect reliability is also examined. Excellent EM performance of Vx/Mx and Vx/Mx+1 for the minimum pitch metal is shown in Figure 17a as an example. Good interconnect thermal stability is illustrated in Figure 17b. The resistance shift percentage of Kevin Rc structures with on-rule and wide metal is found low and negligible after stressed for 500 hours.

Conclusion

The state-of-art 7nm CMOS foundry technology is first introduced with time-to-market solutions for mobile SoC applications. The up-to-date smallest high density SRAM cell is demonstrated with 256Mb fully functional SRAM test-chip and high yield. FinFET transistors are optimized to address both digit and analog design considerations. Compete device and interconnect reliability is examined and improved to meet process qualification criteria for production. The 7nm technology value proposition with competitive PPAC, enabling ~0.43X die size scaling from our 16nm technology, is well illustrated.

References

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[3] S.-Y. Wu et. al., VLSI Tech. Symp., pp. 92-93, 2016.
[4] H.-J. Cho et. al., VLSI Tech. Symp., pp. 12-13, 2016.

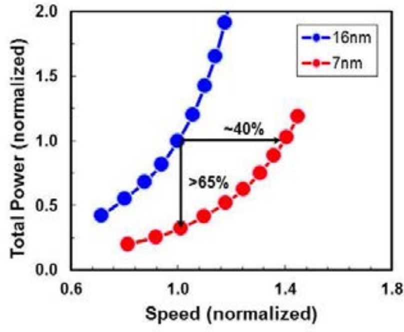


Fig. 1 FOM shows 40% speed gain or >65% power reduction over our 16nm technology.

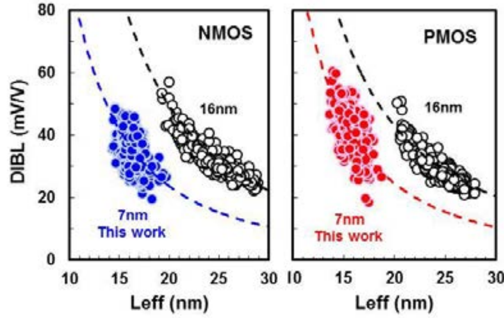


Fig. 2 Device DIBL vs. effective gate length

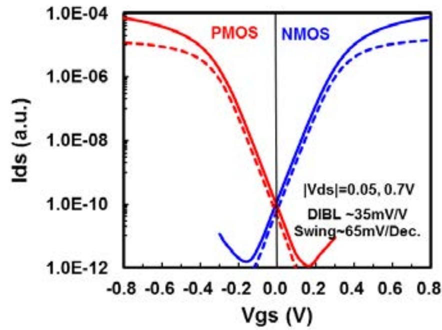


Fig. 3 Typical Id-Vg characteristics of core devices with sub-threshold swing of ~65mV/decade.

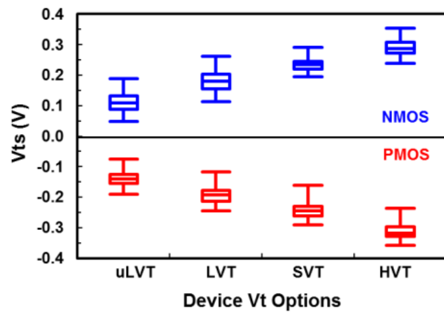


Fig. 4 Multi-Vt device options with Vt range of ~200mV.

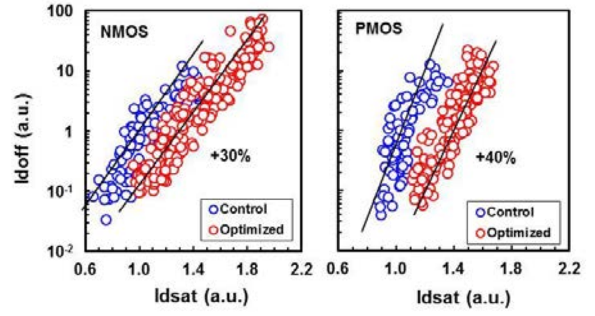


Fig. 5 Device drive current improvement via mobility boost and parasitic resistance reduction.

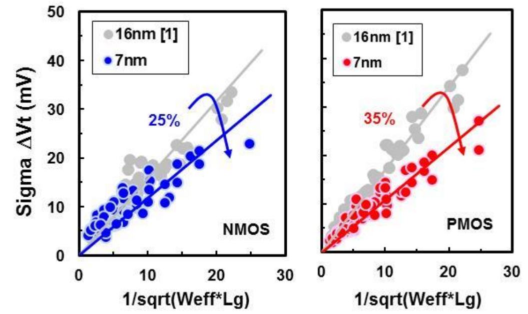


Fig. 6 Device Vt mismatch reduction by 25% and 35% for NMOS and PMOS, respectively.

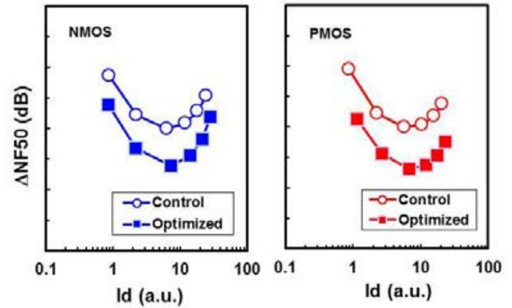


Fig. 7 Device thermal noise improvement through gate resistance reduction.

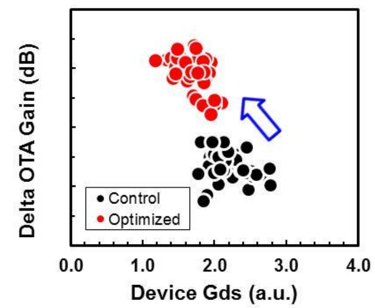


Fig. 8 OTA gain improvement vs. device trans-conductance.

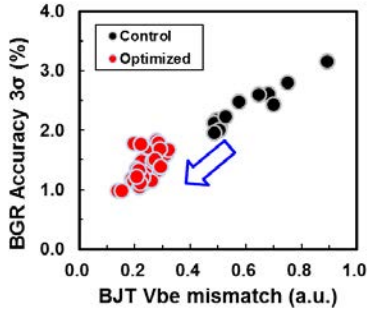


Fig.9 BGR accuracy improvement through BJT mismatch reduction.

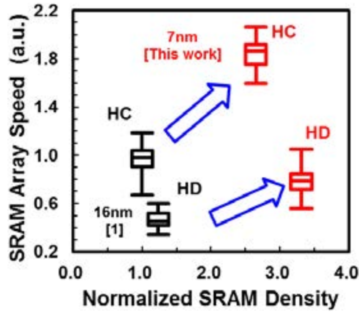


Fig. 10 SRAM array density and array speed improvement.

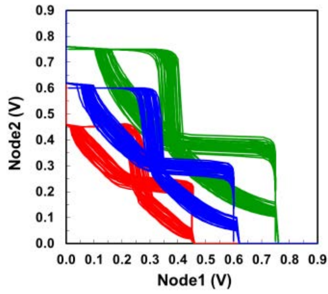


Fig.11 SNM of a 0.027um^2 high density 6-T SRAM cell

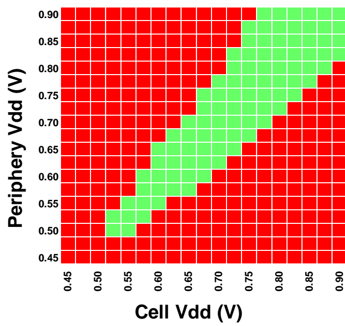


Fig. 12 Shmoo plot of a 0.027um^2 high density 256Mb SRAM macro with full read /write function down to 0.5V.

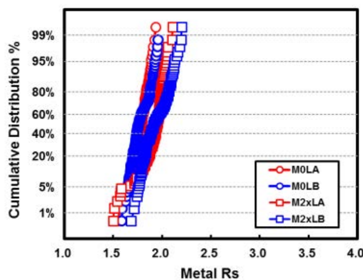
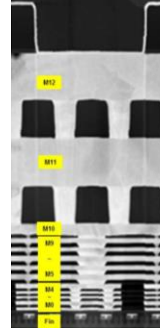


Fig. 13 M0/Mx metal resistance distribution of line A and line B.



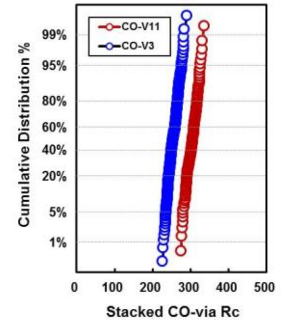


Fig. 14a) A TEM cross-section view of 12-level metal stacks; Fig. 14b) Stacked contact-via Rc distribution.

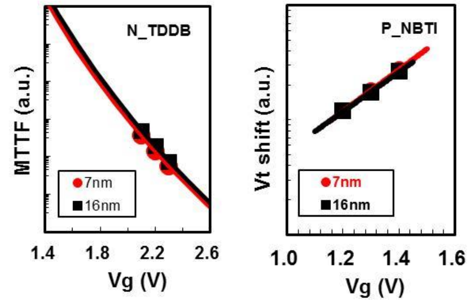


Fig. 15 NMOS TDDB and PMOS NBTI lifetimes.

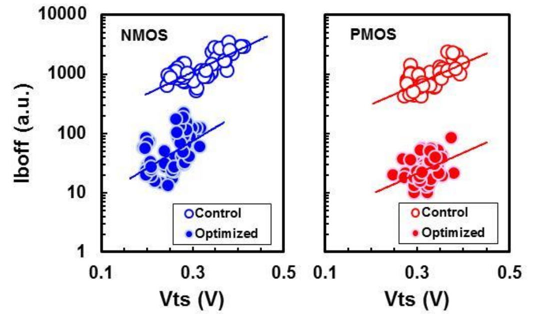


Fig. 16 I/O device Iboff reduction through junction doping profile optimization

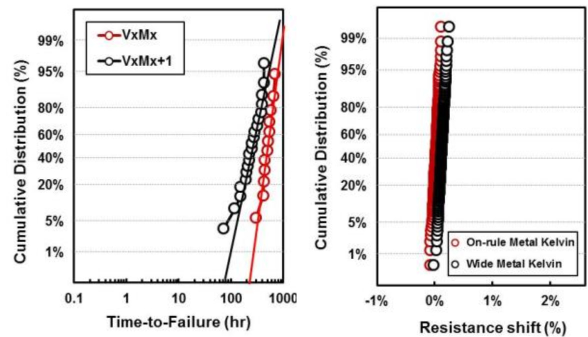


Fig. 17a) EM performance of Vx/Mx & Vx/Mx+1 for min. pitch metal; Fig. 17b) SM performance of kelvin via structures