An Enhanced 16nm CMOS Technology Featuring 2nd Generation FinFET Transistors and Advanced Cu/low-k Interconnect for Low Power and High Performance Applications

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Abstract

Advancing the state-of-the-art 16nm technology reported last year, an enhanced 16nm CMOS technology featuring the second generation FinFET transistors and advanced Cu/low-k interconnect is presented. Core devices are re-optimized to provide additional 15% speed boost or 30% power reduction. Device overdrive capability is also extended by 70mV through reliability enhancement. Superior 128Mb High Density (HD) SRAM Vccmin capability of 450mV is achieved with variability reduction for the first time. Metal capacitance reduction by ~9% is realized with advanced interconnect scheme to enable dynamic power saving.

Introduction

FinFETs with excellent electrostatic and short channel control enable low voltage operation, critical for next generation's low power and high performance applications [1-3]. However, the external parasitic capacitances distributed between fins, in addition to intrinsic device capacitance, increase the dynamic power of circuit operation. This paper presents an enhanced 16nm CMOS technology with effective capacitance reduction in both FinFET transistors and Cu/low-k interconnects for low power and high speed applications. In addition, device reliability is enhanced in order to support maximum operation voltage (Vmax) for additional speed boosts by overdriving the devices. DVFS (Dynamic Voltage Frequency Scaling) range up to 300mV for a product use condition at 85C for 10 year life-time can be realized with technology enhancements.

Process Architecture

Fin patterning and formation on bulk silicon with a 48nm fin pitch is realized using pitch-splitting technique where the fin width is determined by the sidewall thickness of a mandrel. Fin profile and gate profile are carefully co-optimized to balance among the needs to maintain excellent short channel control, to enhance drive current and to reduce parasitic capacitance of the devices. Poly-silicon deposition and gate patterning with a gate pitch of 90nm on the 3-dimensional fin structure is followed by high-K metal gate (HK/MG) RPG process. A dual-gate oxide flow is employed to support core and I/O devices. Gate height is carefully managed in order to provide an optimized combination of gate resistance and gate-to-source/drain (gate-to-S/D) capacitance. Raised source/drain with dual epitaxy process is used and optimized in order to mitigate source/drain (S/D) parasitic resistance. MEOL with tungsten (W) plug provides local routing connected to gate and source/drain. A M1 / Mx metal pitch of 64nm is enabled using advanced patterning scheme, whereas single patterning is adopted for metal pitches of 80nm/90nm and above. Advanced Cu/low-k interconnect process scheme is optimized to provide lower metal capacitance. A planar MiM with high-k dielectrics is also integrated to provide on-chip capacitance >15fF/um^2 for noise reduction.

Transistor Performance

The second generation FinFET transistors are introduced in the enhanced version of our 16nm CMOS technology. Figure of Merits (FOM) based on Inverter, NAND, and NOR circuitry with a fan-out of 3 (F.O.=3) illustrate a 15% speed gain or a 30% total power reduction over our previous reported work [1] as shown in Figure 1. Gate delay (CV/I) of an inverter Ring Oscillator (R.O.) with F.O.=3 measured at different voltages is shown in Figure 2. At 0.8V Vdd, the gate delay is reduced by ~20%. Reduction of gate delays becomes further enhanced as the voltage is further reduced. Superior electrostatic and short channel effect (SCE) of FinFETs are illustrated with competitive DIBL <40mV/V & sub-threshold swing <70mV/dec. [1-4] for core & I/O devices shown in Figure 3.

These values are substantially better than our previously reported 28nm HKMG technology based on planar transistors [5]. Analog characteristics are further enhanced for both core and I/O devices. Figure 4 shows core device intrinsic gain (gm/gds) v.s. analog current (defined as the drain current measured at Vgs=Vt+200mV and Vds=0.5Vdd), whereas I/O device intrinsic gain as a function of gate length achieves significant improvement as shown in Figure 5. Furthermore, the RF cut-off frequency (f_T) and thermal noise have also been improved. Figure 6 shows the improvements in RF cut-off frequency (f_T) of the 2nd Gen. FinFET devices in this work over our previously reported works [1] and [5] measured at a bias of Vgs=0.5V and Vds=0.8V. Figure 7 compares thermal noise of the FinFET devices in this work against those in previous reported works, showing substantial improvement over 28HK/MG devices [5].

SRAM and Interconnect

High Density (HD) and High Current (HC) SRAM cells are further improved to provide speed gain with less standby-leakage current (Isb) over the previous work [1]. Figure 8 compares Isb and SRAM speed of this work with those reported in [1]. As can be seen, a greater than 25% speed gain is realized with lower Isb. This improvement allows the use of a 512 bits per bit-line scheme instead of a 256bits per bit-line scheme to reduce the periphery circuit size. As a result, the macro size for a Gb SRAM macro is reduced by 7~10%. The butterfly curves of the 0.07um^2 HD SRAM cell measured at different voltages are shown in Figure 9, where the excellent cell stability down to 0.4V is clearly demonstrated. The Vccmin of 128Mb SRAM is demonstrated in Figure 10. Vccmin down to 450mV with tight distribution can be clearly observed. In addition, Figure 11 shows the interconnect sheet resistance (Rs) and capacitance (C) of Mx metal with a pitch of 64nm. As can be seen, ~9% metal capacitance reduction has been achieved at the same metal sheet resistance. Via profile is re-optimized in order to maintain the similar Via resistance (Rc) values. Back-end-of-Line (BEOL) defectivity is monitored with a yield tile consists of long metal lines (290m) and 380 million of vias. Stable yields for BEOL as screened by metal line sheet resistance (Mx Rs), metal line leakage current (Mx LK) and Via resistance (Via Rc) are demonstrated in Figure 12.

Device Reliability

Device reliability of the second generation FinFET like time-dependent-dielectric-breakdown (TDDB), bias-temperature-instabilities (BTI) and hot carrier injection (HCI) are further improved and characterized to maximize the performance gain of the technology. With careful post high-k/MG thermal optimization, TDDB and BTI for both NMOS and PMOS are improved. Figure 13 shows the improved the Mean-time-to-failure (MTTF) of TDDB for NMOS and PMOS in this work versus those in the previous work [1], Figure 14 shows improved BTI with reduced threshold voltage (Vt) shifts under various stress voltages for core NMOS and PMOS. High quality I/O gate oxide/high-k dielectric enables good TDDB and BTI for I/O devices. In addition, hot carrier immunity is also addressed with junction doping profile optimization for both core and I/O devices. Figure 15 shows improved Vt shift from HCI as a function of different voltages (Vdd). Overall the maximum operation voltage (Vmax) of core devices is raised by 70mV through reliability enhancement. Figure 16 compares speed and leakage power of a representative ring oscillator (R.O.) at the nominal bias voltage, at the Vmax of the previous work [1] and at the Vmax of this work. The increase in Vmax of this technology is found to translate into a 10% speed increase over the speed at the maximum operation voltage of work [1] as illustrated in Figure 16.

Conclusion

An enhanced second generation 16nm FinFET CMOS foundry technology with lower power, higher performance and smaller SRAM macro size and lower SRAM Vccmin is developed based on improved capacitance, better SRAM speed, lower Isb and enhanced SRAM cell stability. Reliability robustness and variability reduction provide an additional 10% performance gain at the Vmax and wider manufacturing margins for volume production.

References

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[3] C.-H. Jan et. al., IEDM Tech. Dig., pp. 44-47, 2012
[4] Q. Liu et al., IEDM Tech. Dig., pp. 228-231, 2013
[5] S. Yang et al., CICC, pp. 1-5, 2011

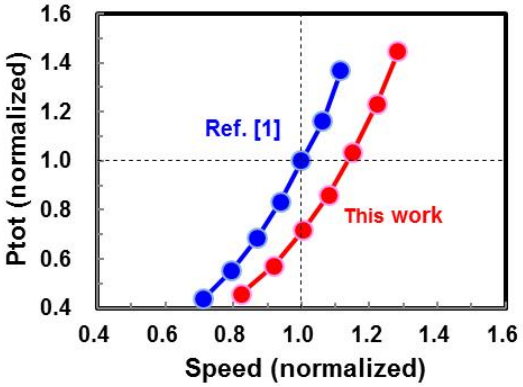

Fig. 1 FOM shows 15% speed gain or 30% power reduction.

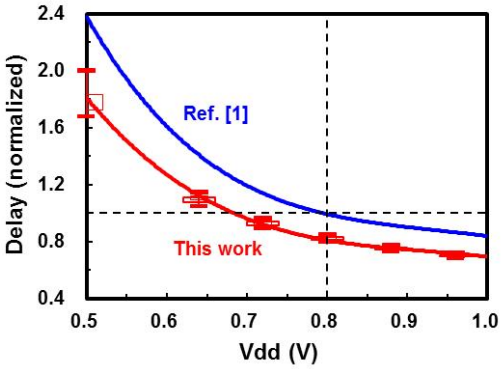

Fig. 2 CV/I of an inverter R.O. (F.O.=3) at different Vdd.

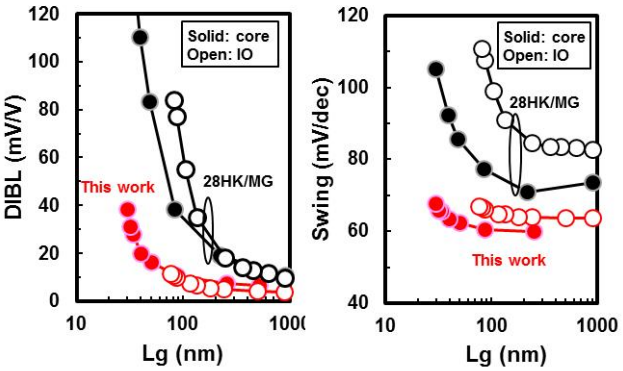

Fig. 3 Superior FinFET device DIBL and sub-threshold swing.

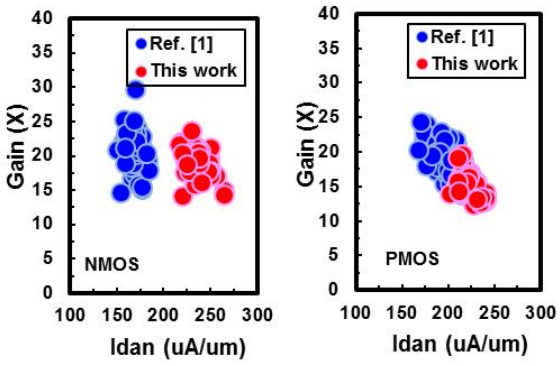

Fig. 4 Core device intrinsic gain (gm/gds) vs.drain current at Vgs=Vt+200mV and Vds=0.5*Vdd.

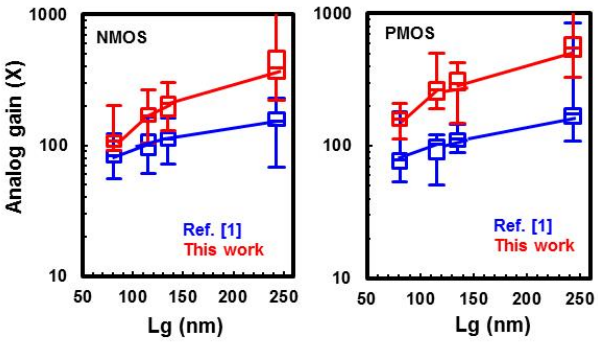

Fig. 5 Improved I/O device intrinsic gain (gm/gds) vs. Lg.

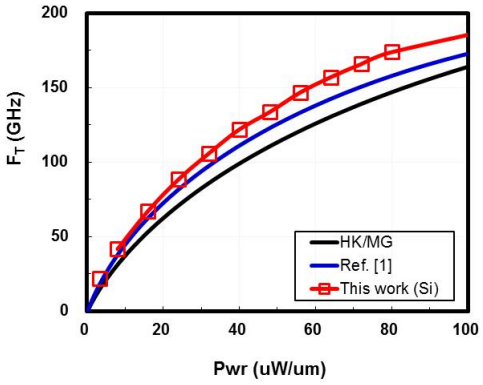

Fig. 6 NMOS RF cut-off frequency (f_T) vs. power at Vgs=0.5V and Vds=0.8V.

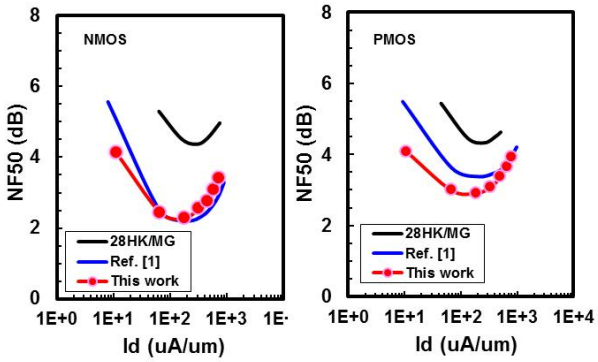

Fig. 7 FinFET devices achieve lower thermal noise than 28HK/MG.

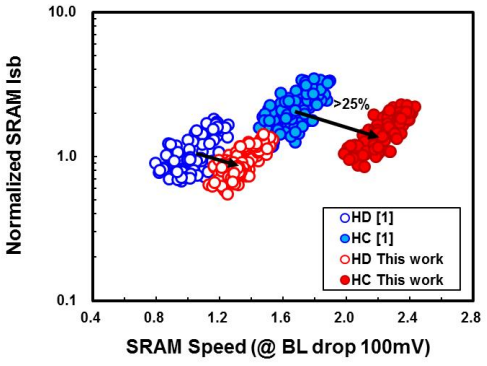

Fig. 8 HC/HD SRAM cell speed is boosted by >25% with less Isb.

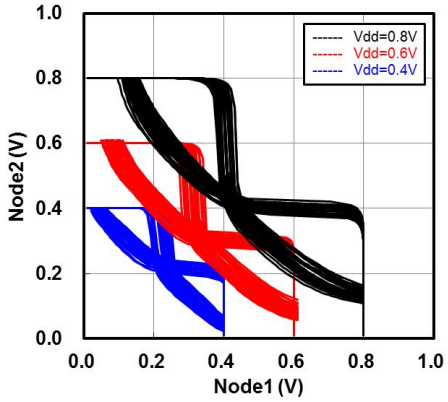

Fig.9 SNM of 0.07um^2 HD SRAM cell is illustrated down to 0.4V.

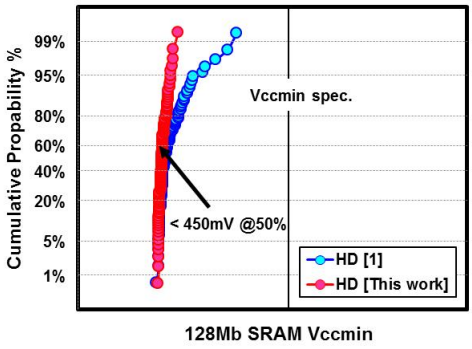

Fig. 10 128Mb HD SRAM Vccmin capability of 450mV is achieved.

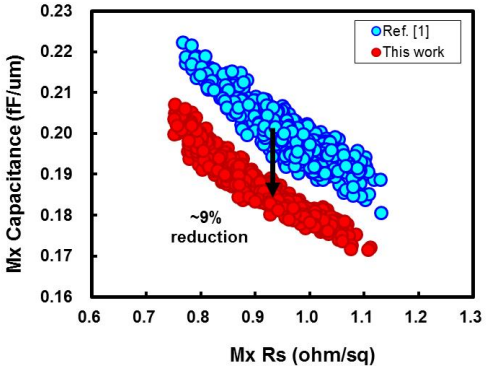

Fig.11 Metal capacitance is reduced by ~9% for Mx pitch of 64nm.

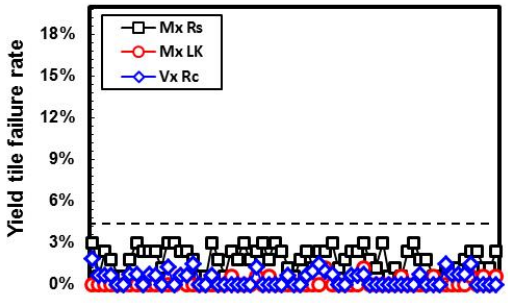

Fig. 12 Stable BEOL yield tile consists of metal Rs and via Rc.

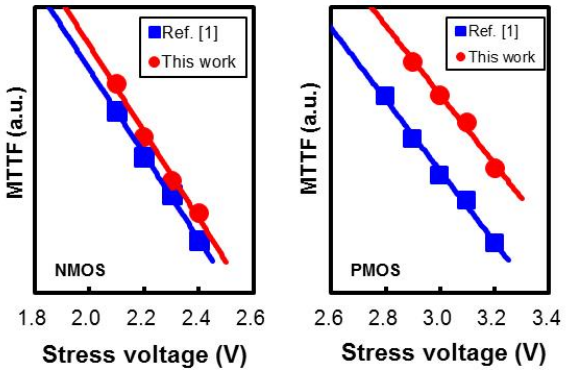

Fig. 13 Improved core NMOS and PMOS TDDB in this work.

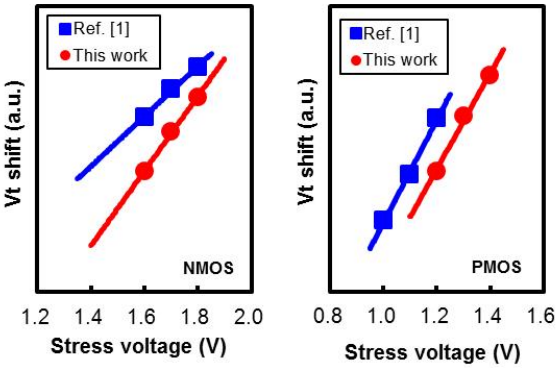

Fig. 14 Improved core device NBTI and PBTI in this work.

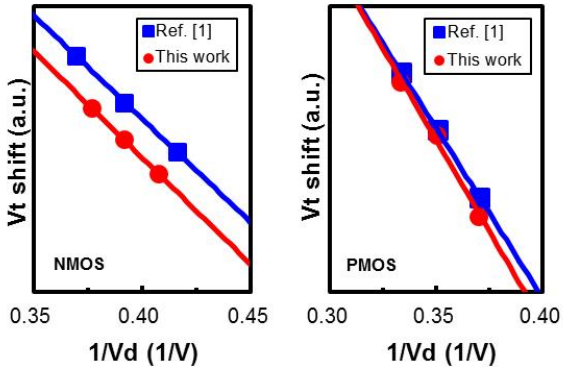

Fig. 15 I/O NMOS and PMOS HCI are improved by S/D junction opt.

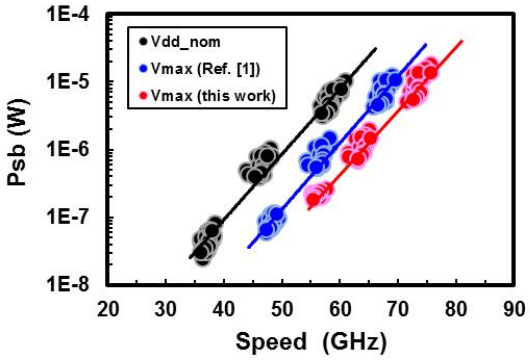

Fig. 16 The improved Vmax provides additional 10% R.O. speed gain.