A 14nm Logic Technology Featuring 2nd-Generation FinFET Transistors, Air-Gapped Interconnects, Self-Aligned Double Patterning and a 0.0588μm² SRAM cell size

S. Natarajan, M. Agostinelli*, S. Akbar, M. Bost, A. Bowonder, V. Chikarmane, S. Chouksey, A. Dasgupta, K. Fischer, Q. Fu, T. Ghani, M. Giles**, S. Govindaraju, R. Grover, W. Han, D. Hanken, E. Haralson, M. Haran, M. Heckscher, R. Heussner, P. Jain, R. James, R. Jhaveri, I. Jin, H. Kam, E. Karl, C. Kenyon, M. Liu, Y. Luo, R. Mehandru**, S. Morarka**, L. Neiberg, P. Packan, A. Paliwal, C. Parker, P. Patel, R. Patel, C. Pelto, L. Pipes, P. Plekhanov, M. Prince, S. Rajamani, J. Sandford, B. Sell, S. Sivakumar, P. Smith, B. Song, K. Tone, T. Troeger, J. Wiedemer, M. Yang, K. Zhang

Logic Technology Development, * Quality and Reliability Engineering, ** DTS, Intel Corporation.
Phone: (503) 613-8029; Email: sanjay.natarajan@intel.com

ABSTRACT

A 14nm logic technology using 2nd-generation FinFET transistors with a novel subfin doping technique, self-aligned double patterning (SADP) for critical patterning layers, and air-gapped interconnects at performance-critical layers is described. The transistors feature rectangular fins with 8nm fin width and 42nm fin height, 4th generation high-k metal gate, and 6th-generation strained silicon, resulting in the highest drive currents yet reported for 14nm technology. This technology is in high-volume manufacturing.

INTRODUCTION

Relentless focus on transistor scaling and Moore's Law has led to ever-higher transistor performance and density, translating into tremendous increases in microprocessor functionality and performance. Traditional scaling had reached limitations of electrostatics and short-channel effects, threatening the continuance of Moore's Law. 22nm tri-gate transistors[1] broke through some of these scaling barriers. This paper reports on a 14nm process technology, including a 2nd generation FinFET architecture, which provides industry-leading transistor performance and density.

KEY DESIGN RULES & TECHNOLOGY FEATURES

Table 1 summarizes key design rules and scale factors for the 14nm node compared to 22nm node[1]. Fin pitch, a key measure of transistor density for FinFETs, is scaled to 42nm, maintaining 0.7x scaling trend from 22nm[1]. Contacted gate pitch is scaled to 70nm. Interconnect pitches are as low as 52nm and scaled between 0.65x and 0.78x. SADP with 193nm immersion lithography is used at critical patterning layers to enable aggressive design rule scaling. Fig. 1 shows the scaling trend of contacted gate pitch multiplied by metal pitch (as a proxy for density) for the past four Intel generations as well as published industry data. The Intel 14nm process continues to maintain the historical trend of density improvement per generation.

TRANSISTOR PERFORMANCE AND VARIATION

Lgate scaling from 26nm in the 22nm node (from conference presentation from [1]) to 20nm in the 14nm node is enabled by fin profile optimization and a novel subfin doping technique. Subfin doping of high performance transistors is achieved through solid-source doping to enable better optimization of punch-through stopper dopants. Fig. 2 shows transistor fin-cut and gate-cut images. NMOS and PMOS Idsat/Ioff and Idlin/Ioff curves are shown in Figs. 3 and 4. At 0.7V Vdd, 10nA/um Ioff, 42nm fin pitch and 70nm contacted gate pitch, saturated drive currents are 1.04mA/um (all drive currents are per-micron of layout width) for both NMOS and PMOS. Idsat is improved 15% for NMOS and 41% for PMOS over 22nm[1], and these are the best drive currents reported to-date for 14nm technology. NMOS and PMOS linear drive currents are 0.237mA/um and 0.203mA/um, respectively, at 10nA/um Ioff, Vgs=0.7V, and Vds=50mV. These represent an improvement of 30% for NMOS and 38% for PMOS over 22nm[1]. Transistor I-V and sub-threshold characteristics are shown in Figs. 5 and 6. Sub-threshold slopes are maintained at ~65mV/decade. DIBL is ~60mV/V and ~75 mV/V for NMOS and PMOS, respectively. Random variation data for minimum-sized devices for multiple Intel process technology generations is shown in Fig. 7. The trend in increasing σVt due to Z scaling for planar MOSFETs was reversed in 22nm. With optimizations in fin profile and doping, σVt was reduced in 14nm by a factor of nearly 2x, enabling significant improvement in product Vmin.

RELIABILITY

Optimization of the high-k + metal-gate stack yields excellent reliability characteristics. Fig. 8 shows PMOS and NMOS TDDB, respectively. Both show a clear improvement relative to 22nm. Fig. 9 shows superior aging compared to 22nm as measured by reduced Vccmin degradation under stress.

INTERCONNECTS

10 layers of the 13-layer Cu interconnect stack are shown in Fig. 10. Low-k CDO dielectrics are used on 8 layers. Lower-layer metal pitches are scaled aggressively relative to [1], by as much as 0.65x. Fig. 11 shows two layers of air-gapped interconnect, used to provide improved capacitance at performance-critical layers. Air gaps are used at 80nm and 160nm minimum pitch layers and provide a 17% improvement in capacitance. A thick top metal is used for improved on-die power distribution.

SRAM, PRODUCT AND YIELD

The 14nm test chip includes a 140Mbit SRAM featuring a 0.0588μm² bitcell (Fig. 12) with an array density of 11.6Mb/mm². This process is now in high-volume manufacturing, producing a family of processors using the Broadwell microarchitecture (Fig. 13). Yield in production is in a healthy range for high-volume manufacturing.

CONCLUSIONS

We have demonstrated an industry-leading 14nm CMOS technology with excellent transistor and interconnect performance and aggressive design rule scaling. The process features 2nd generation FinFETs with optimized fin profiles and a novel sub-fin doping technique, 52nm minimum pitch interconnects formed with SADP, air-gap interconnects at performance-critical layers, and aggressive design rule scaling from the 22nm generation to provide a true 14nm technology. We have shown a high-performance, high-density SRAM featuring 0.0588μm² cell size fabricated using all 14nm process features. This process is in high-volume manufacturing.

REFERENCES

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4. H. Shang, et al., *Symp. VLSI Tech Dig.*, p.129, 2012.
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Layer	Pitch (nm)	Scale Factor to [1]
Fin	42	0.70
Contacted Gate Pitch	70	0.78
Metal 0	56	N/A
Metal 1	70	0.78
Metal 2	52	0.65

Table 1: Layer Pitches

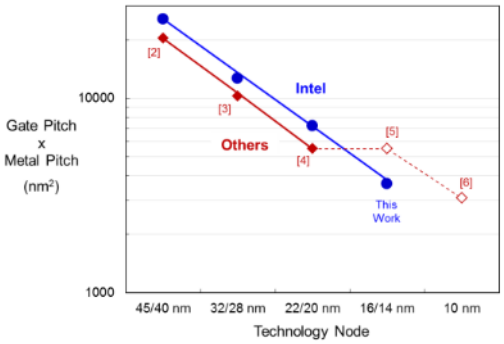

Figure 1: Multi-Generation Scaling Trend

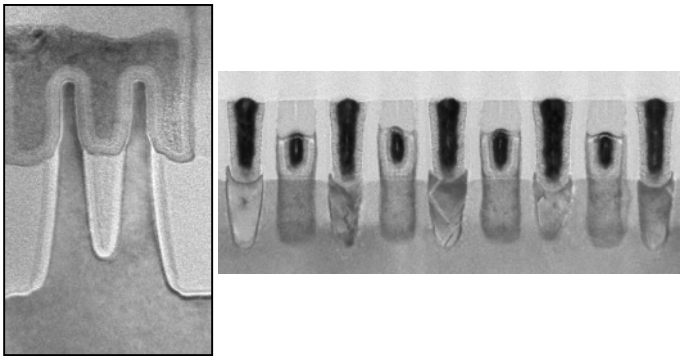

Figure 2: Transistor Fin and Gate-Cut Images

(not same scale)

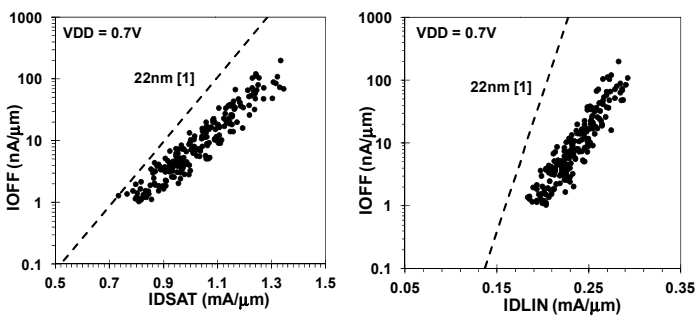

Figure 3: NMOS Idsat and Idlin curves

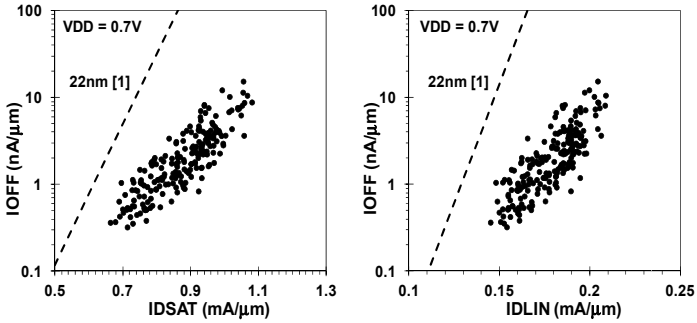

Figure 4: PMOS Idsat and Idlin curves

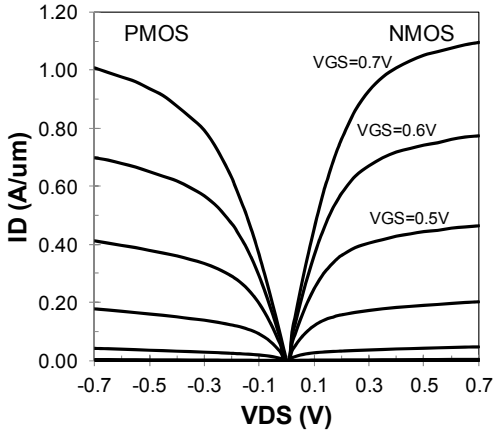

Figure 5: Transistor I-V Curves

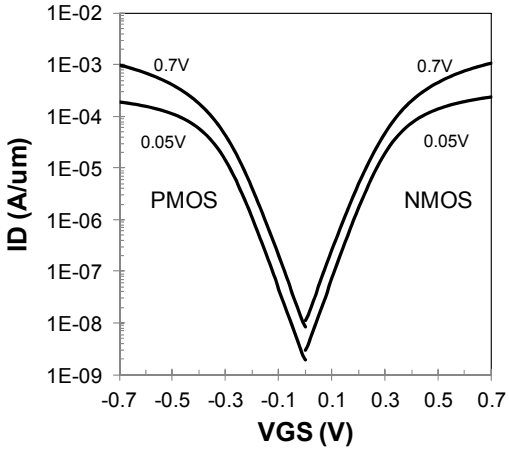

Figure 6: Subthreshold Curves

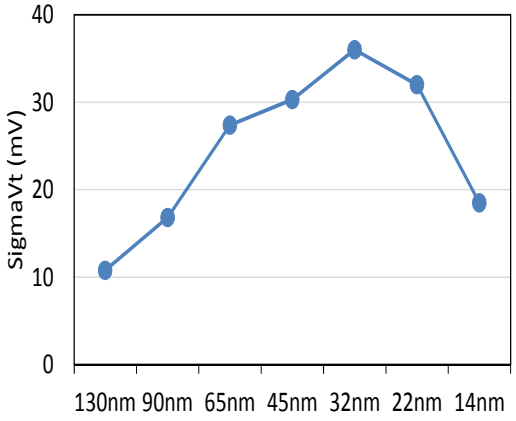

Figure 7: Random Varation Trend (σVt)

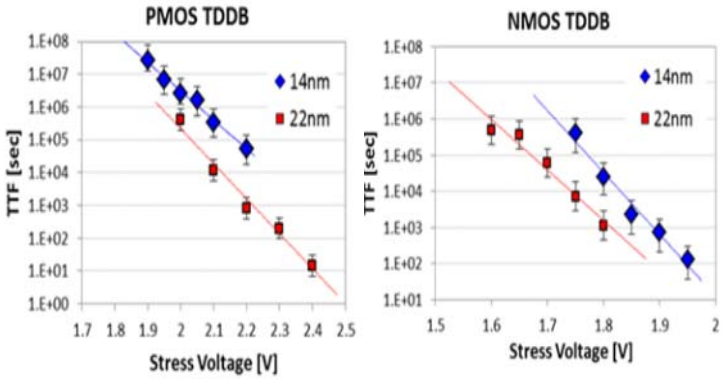

Figure 8: PMOS and NMOS TDDB

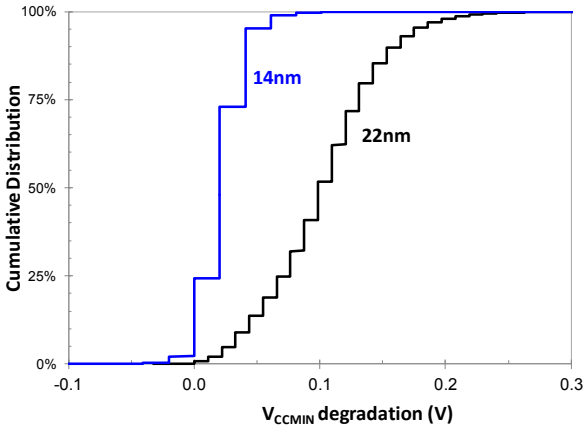

Figure 9: SRAM Aging Behavior

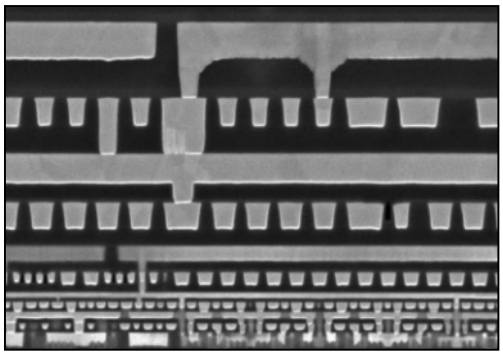

Figure 10: Interconnect Stack

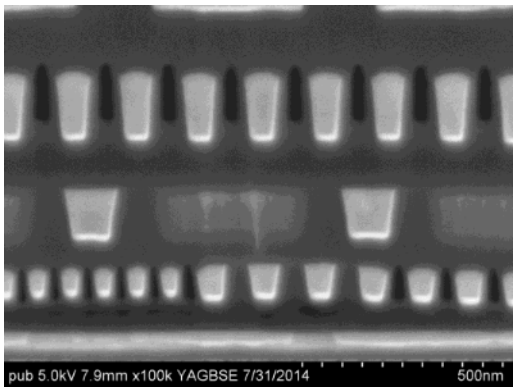

Figure 11: Air-Gapped Interconnects

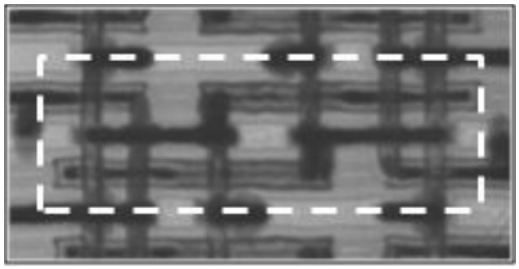

Figure 12: SRAM Bitcell

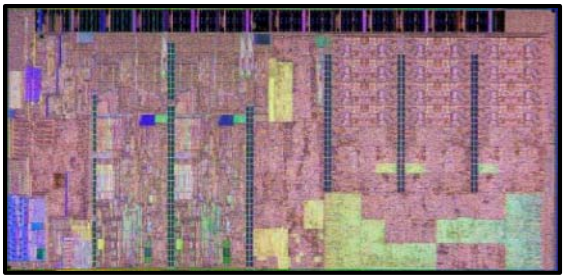

Figure 13: Broadwell Die Photo