

廖洺漢

著作目錄

期刊論文

1. M.-H. Liao*, C.-P. Hsieh, and C.-C. Lee* (2017, Jul). The investigation of self-heating effect on Si_{1-x}Ge_x FinFETs with different device structures, Ge concentration, and operated voltages. *AIP Advances*, Vol. 7, p. 055105. 本人為第一作者、通訊作者.
2. M.-H. Liao*, H.-I. Huang, and C.-C. Chuang (2017, Jun). Performance Enhancement for the Triboelectric Energy Harvester by using interfacial micro-dome array structures. *Appl. Phys. Lett.*, Vol. 110, p. 153901. 本人為第一作者、通訊作者.
3. Van Su Luong, Yu-Hsin Su, Chih-Cheng Lu, Jen-Tzong Jeng, Jen-Hwa Hsu, M.-H. Liao, Jong-Ching Wu, Meng-Huang Lai, and Ching-Ray Chang (2017, May). Planarization, Fabrication and Characterization of Three-dimensional Magnetic Field Sensors. *IEEE Trans. on Nanotech.*, Vol. 99, p. 1.
4. M.-H. Liao*, C.-P. Hsieh, and C.-C. Lee* (2017, Feb). The systematic investigation of self-heating effect on CMOS Logic transistors from 20 nm to 5 nm technology nodes by experimental thermo-electric measurements and finite element modeling. *IEEE Trans. on Electron Devices*, Vol. 64(2), pp. 646-648. 本人為第一作者、通訊作者.
5. C. C. Lee*, H.-W. Hsu, and M.-H. Liao* (2017, Jan). The effect of CESL and dummy poly gate for n-type MOSFETs with short Si_{0.75}Ge_{0.25} channel. *Vacuum*, Vol. 140, p. 66. 本人為通訊作者.
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8. P.-G. Chen, M. Tang, M.-H. Liao and M. H. Lee (2017, Jan).

In_{0.18}Al_{0.82}N/AlN/GaN HEMT on Si with Hybrid Ohmic and Schottky Source/Drain Solid State Electronics. *Solid State Electronics*, Vol. 129, pp. 206-209.

9. C. C. Lee*, S. W. Cheng, C. P. Hsieh, M.-H. Liao*, and Y. H. Guo (2016, Sep). Comprehensive Investigation on Array-Type Dummy Active Diffused Region and Gate Geometries Using Narrow NMOSFETs with SiC S/D Stressors. *International Journal of Nanotechnology*, Vol. 13, No. 7, p. 492.
10. C. Liu, P.-G. Chen, M.-J. Xie, S.-N. Liu, J.-W. Lee, S.-J. Huang, S. Liu, Y.-S. Chen, H.-Y. Lee, M.-H. Liao, P.-S. Chen, and M.-H. Lee (2016, Mar). Simulation-based study of negative capacitance double gate tunnel field effect transistor with ferroelectric gate stack. *Japanese Journal of Appl. Phys*, Vol. 55, p. 04EB08, 2016.
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15. M.-H. Liao and P.-G. Chen (2015, Oct). The demonstration of the Si nano-tube device with the promising short channel control. *J. Appl. Phys.*, Vol. 118, p. 135705, 2015. MOST 103-2221-E-002-215-MY3. 本人為第一作者、通訊作者。
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experimental process support from NDL is also highly appreciated. The support from the Big League Program with TSMC is also highly appreciated.

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20. M.-H. Liao and P.-G. Chen (2015, Apr). The demonstration of dislocation-stress memorization technique stressor on Si n-FinFETs. *IEEE Transactions on Nanotechnology*, Vol. 14(4), p. 657, 2015.. MOST 102-2218-E-002-003. 本人為第一作者、通訊作者.
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26. M.-H. Liao and P.-G. Chen (2013, Aug). Experimental demonstration for ultra-low on-resistance in raised source/drain In_{0.53}Ga_{0.47}As QW-MOSFETs with implant-free process. *J. Phys. D: Appl. Phys.*. 本人為第一作者、通訊作者.
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研討會論文

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4. M.-H. Liao, P. G. Chen, S. C. Huang, S. C. Kao, C. X. Hung, K. H. Liu, C. Lien,
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5. M.-H. Liao, S. C. Huang, C. Y. Liu, P. G. Chen, S. C. Kao, and C. Lien (2014,
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performance on Ge (100) n-FETs by the novel magnetic gate stack scheme
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本人為第一作者、通訊作者. 2014 Symposium on VLSI Technology.