LEADING AT THE EDGE

TECHNOLOGY AND MANUFACTURING DAY

DISCLOSURES

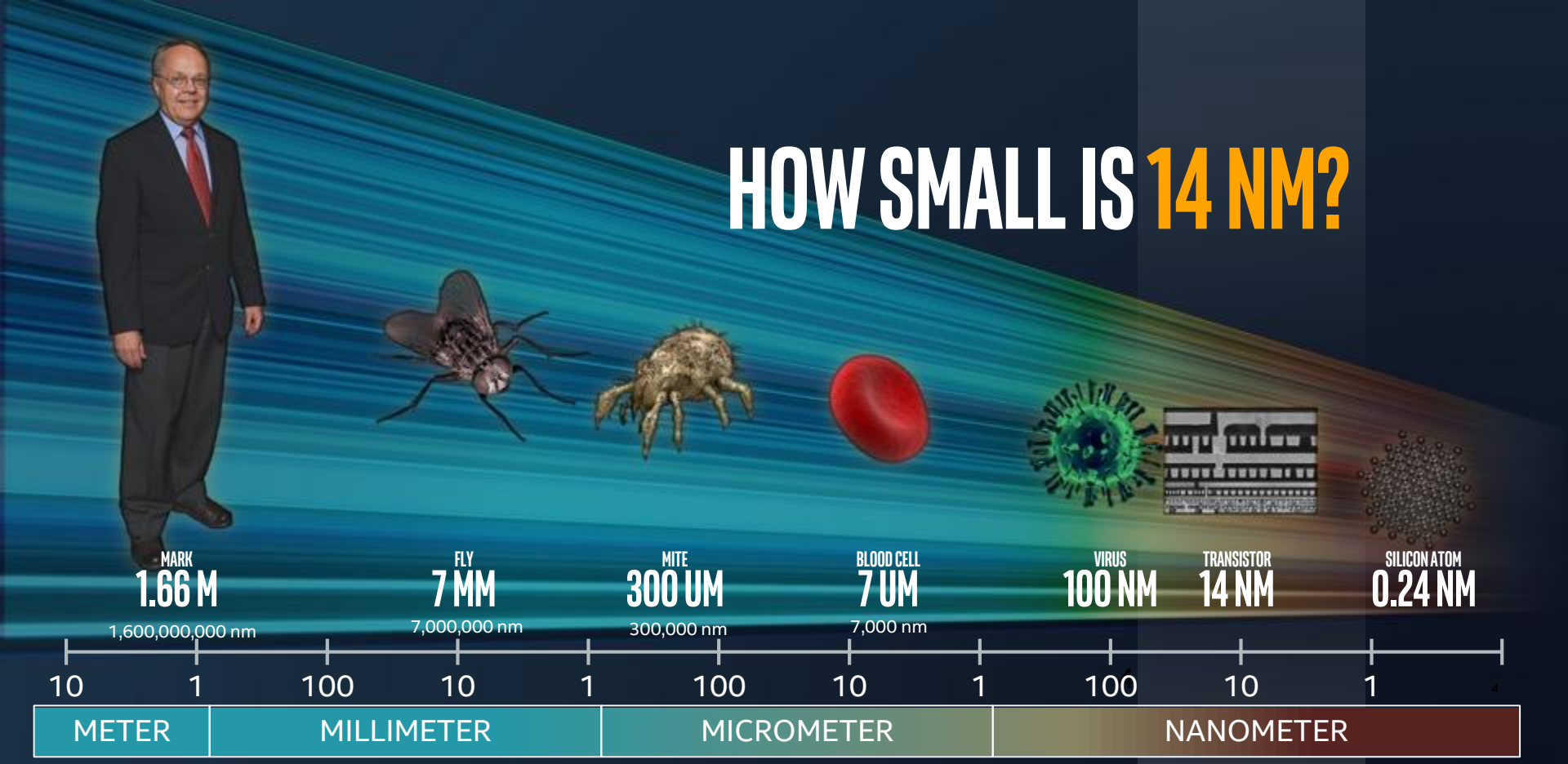
Intel Technology and Manufacturing Day 2017 occurs during Intel's "Quiet Period," before Intel announces its 2017 first quarter financial and operating results. Therefore, presenters will not be addressing first quarter information during this year's program.

Statements in this presentation that refer to forecasts, future plans and expectations are forward-looking statements that involve a number of risks and uncertainties. Words such as "anticipates," "expects," "intends," "goals," "plans," "believes," "seeks," "estimates," "continues," "may," "will," "would," "should," "could," and variations of such words and similar expressions are intended to identify such forward-looking statements. Statements that refer to or are based on projections, uncertain events or assumptions also identify forward-looking statements. Such statements are based on management's expectations as of March 28, 2017, and involve many risks and uncertainties that could cause actual results to differ materially from those expressed or implied in these forward-looking statements. Important factors that could cause actual results to differ materially from the company's expectations are set forth in Intel's earnings release dated January 26, 2017, which is included as an exhibit to Intel's Form 8-K furnished to the SEC on such date. Additional information regarding these and other factors that could affect Intel's results is included in Intel's SEC filings, including the company's most recent reports on Forms 10-K, 10-Q and 8-K reports may be obtained by visiting our Investor Relations website at www.intc.com or the SEC's website at www.sec.gov.

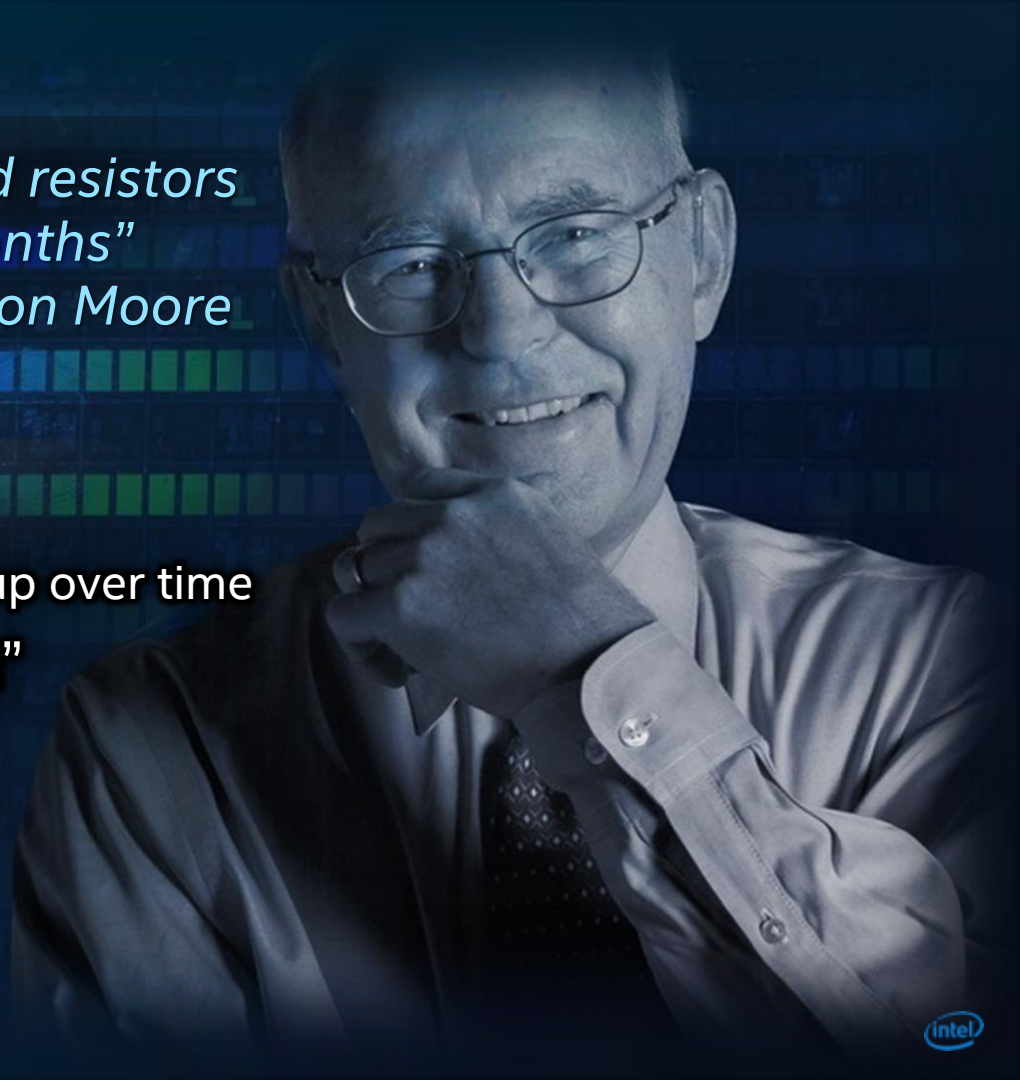
STRATEGY OVERVIEW

STACY J. SMITH
Executive Vice President
Manufacturing, Operations and Sales

HOW SMALL IS 14 NM?



"The number of transistors and resistors on a chip doubles every 24 months"
-Gordon Moore



Two Implications:

1. Cost per square millimeter goes up over time
2. Doubling of transistors = "Scaling"
   - Improves performance
   - Cost per transistor declines

WHAT IF MOORE'S LAW IS APPLIED TO…

TRANSPORTATION?

We could travel to the Sun on a single gallon

AGRICULTURAL PRODUCTIVITY?

We could feed the world's population with 1km^2 of land

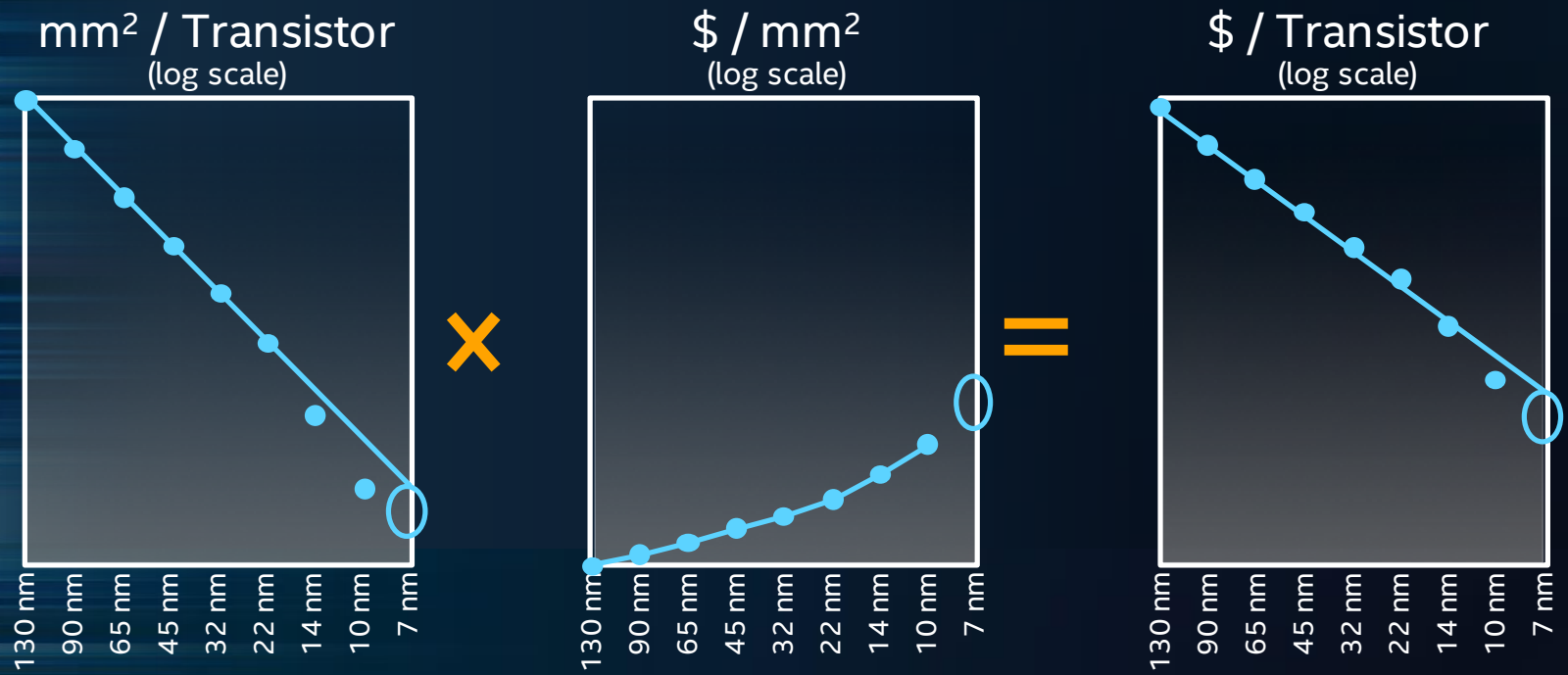
SPACE TRAVEL?

We could travel at 300x light-speed

Source: Intel estimates.

IS MOORE'S LAW DEAD?

IS MOORE'S LAW DEAD? NO!



10 nm and 7 nm forecasts are Intel estimates, based upon current expectations and available information.
Source: Intel

The time between nodes has lengthened…

ARE YOU GETTING THE SAME MOORE'S LAW BENEFIT?

YES!

Because we are getting more scaling

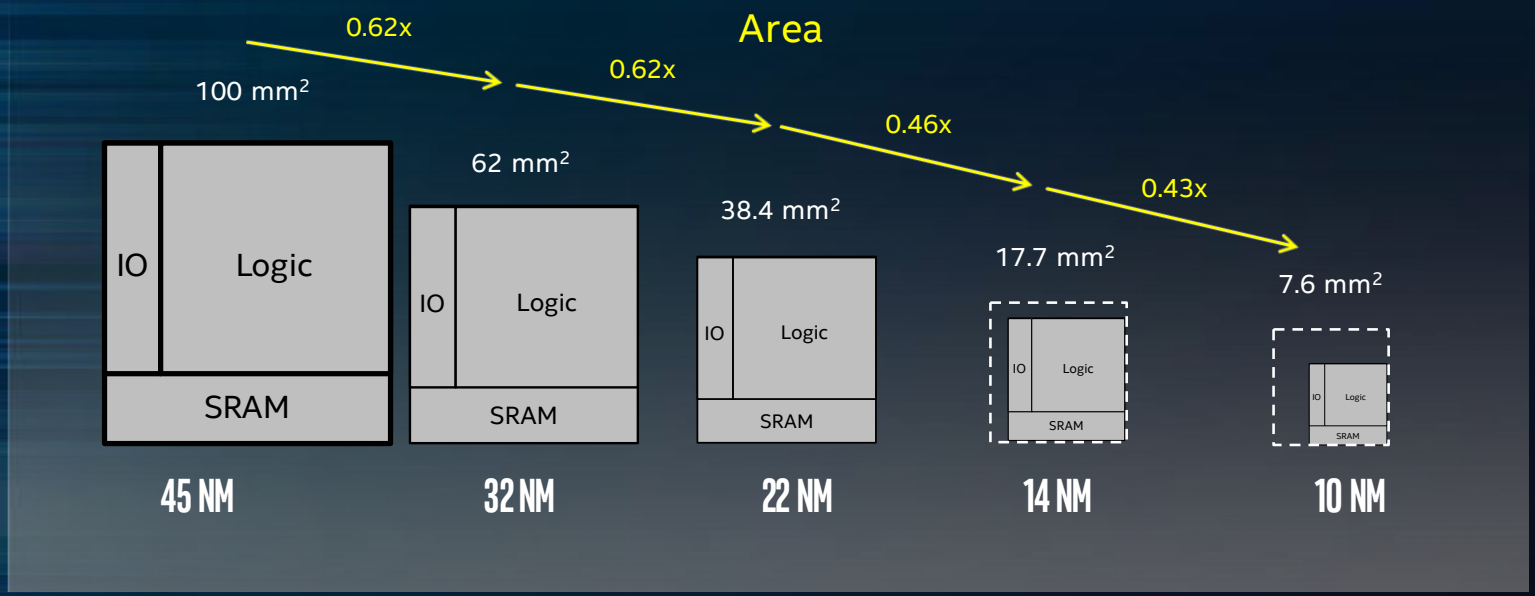
WE ARE HYPER SCALING

(on 14 nm & 10 nm)

Hyper scaling enables us to achieve accelerated density improvement

Intra-node optimizations enable an annual cadence of product enhancements

MICROPROCESSOR DIE AREA SCALING



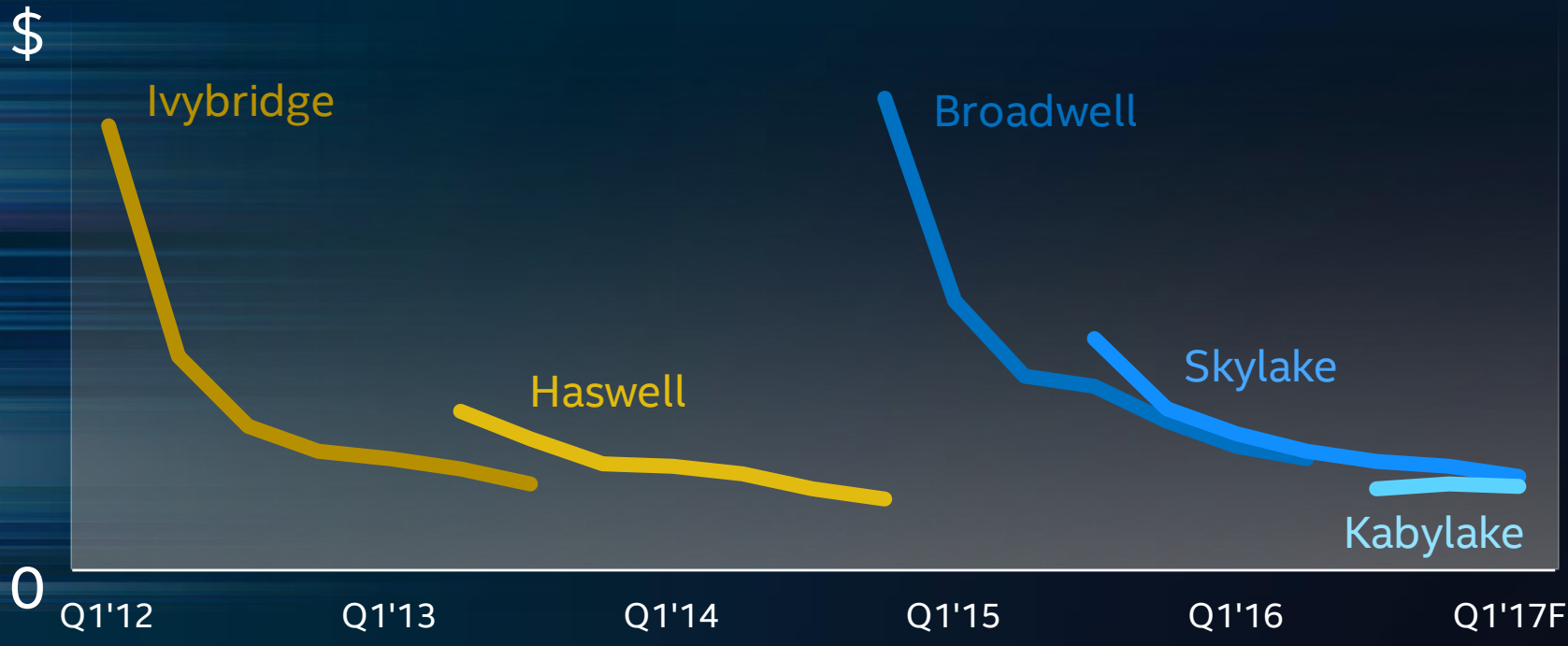
Hyper scaling delivers 0.46–0.43x die area scaling on 14 nm and 10 nm

10 nm forecast is an Intel estimate, based upon current expectations and available information.
Source: Intel

MOORE'S LAW TRANSLATES TO LOWER PRODUCT COSTS

22 nm & 14 nm Client Cost Curves

(Launch + 5 quarters)

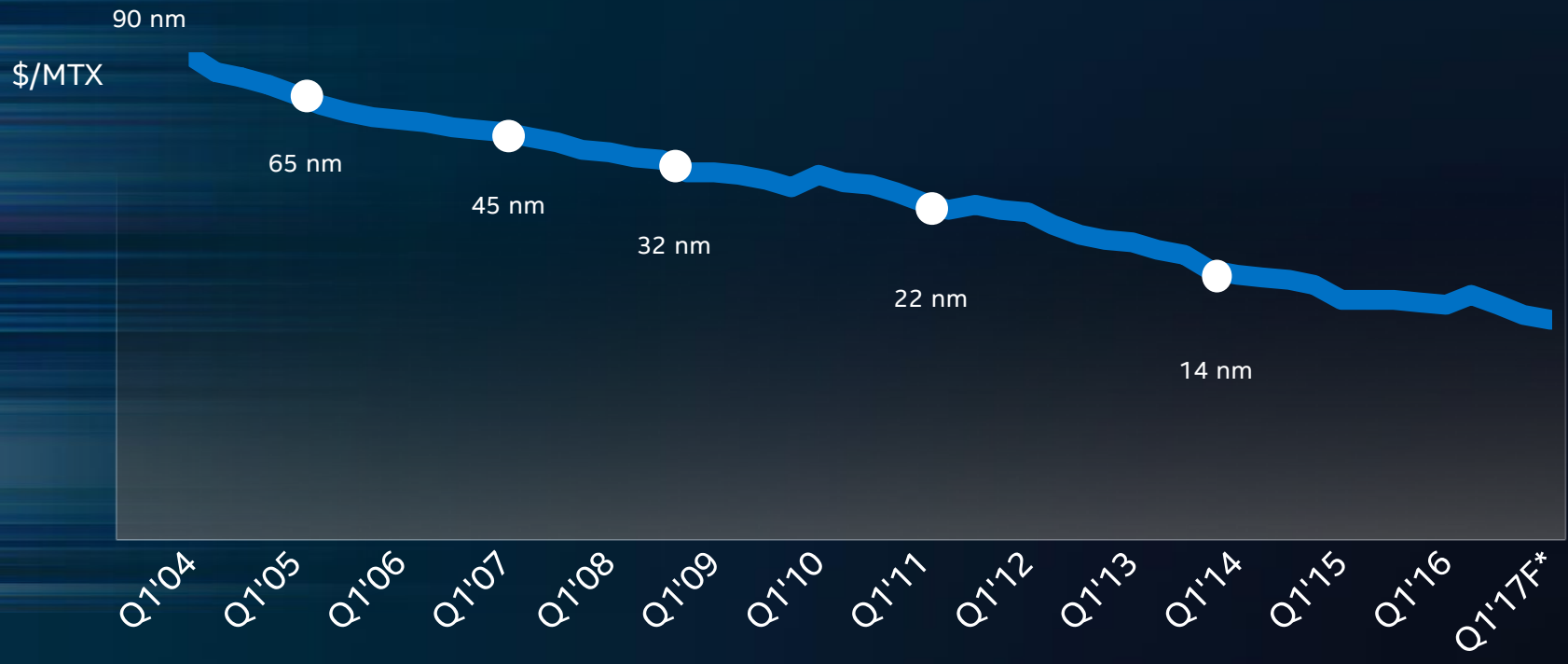


*Q1'17 forecast is an Intel estimate, based upon current expectations and available information.
Source: Intel

MOORE'S LAW IN ACTION…

PC CPU Weighted Average Cost Per Transistor ($/MTX)

(log scale normalized to 90 nm)

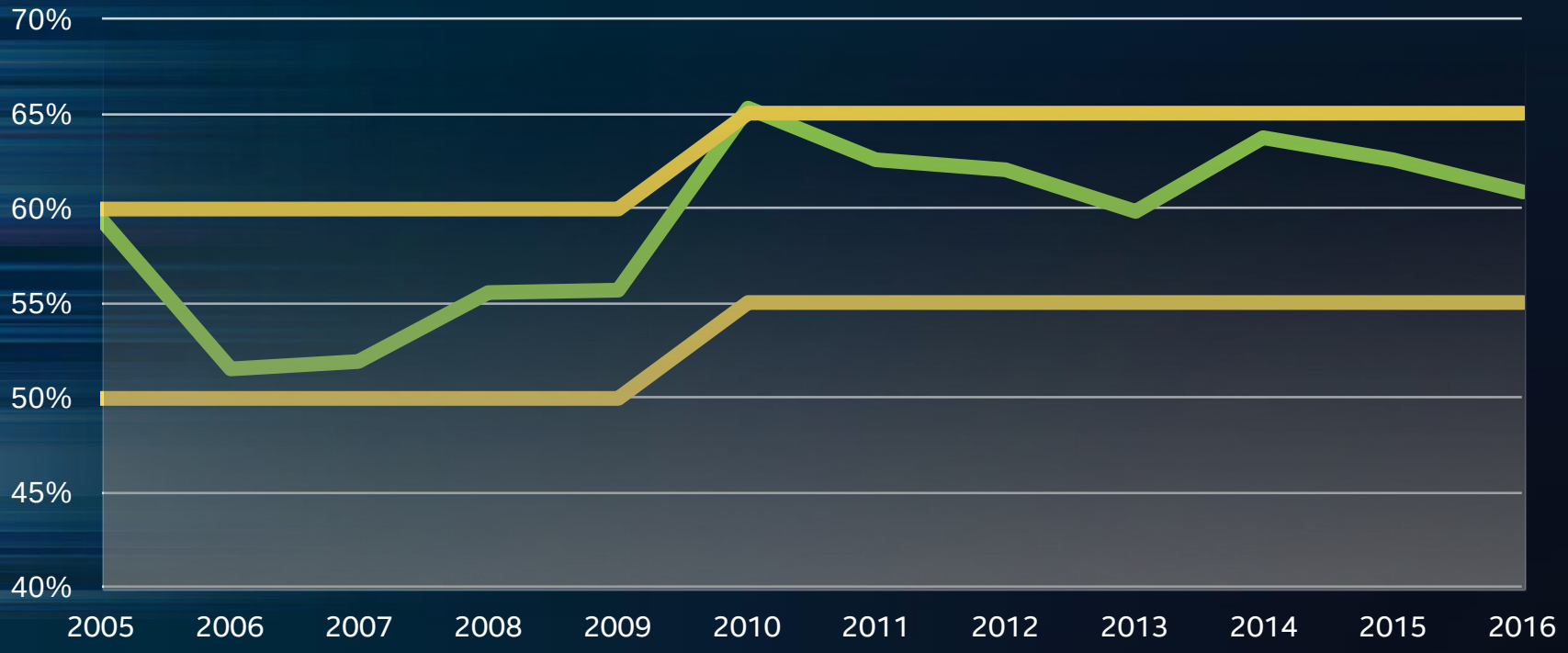


*Q1'17 forecast is an Intel estimate, based upon current expectations and available information.

Source: Intel

GROSS MARGINS

Gross Margin % Annual 2005 - 2016



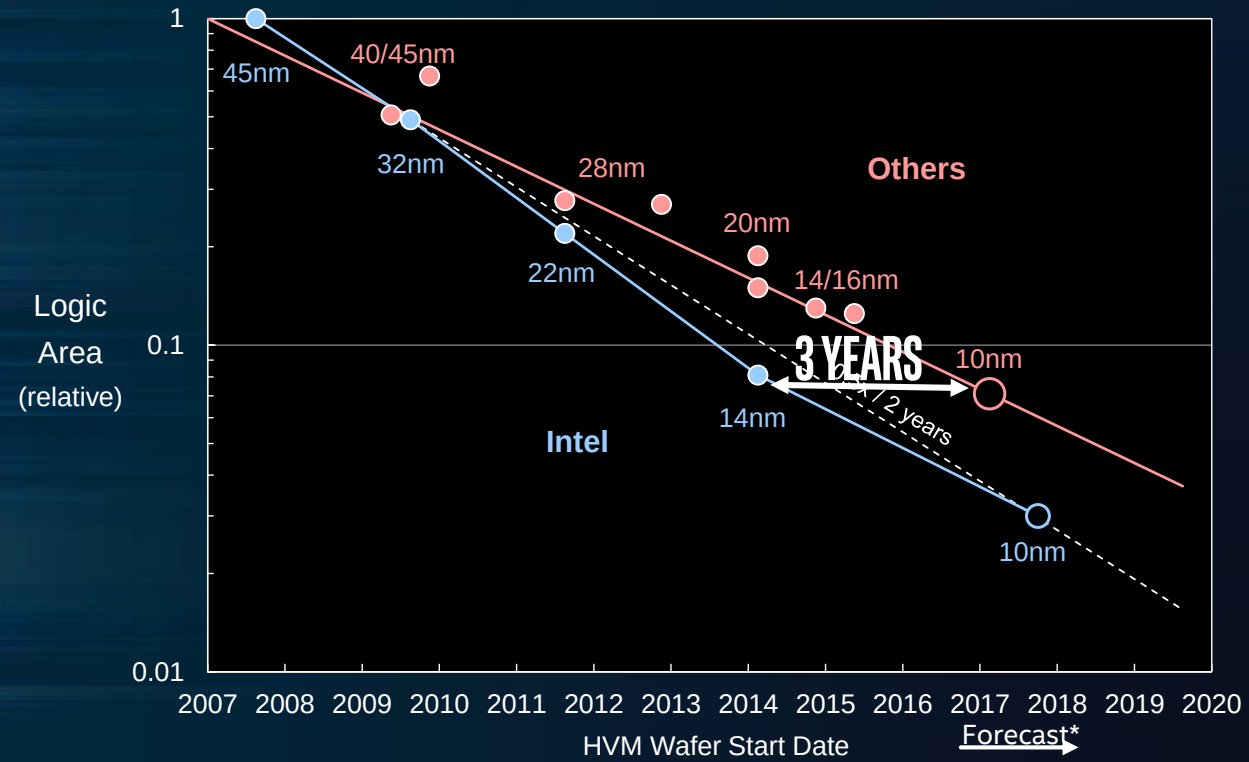
Source: Intel

Competitors are announcing10nm this year…

HAVE YOU LOST YOUR LEAD?

HAVE YOU LOST YOUR LEAD? NO!

14 NM IS ~3 YEARS AHEAD



*Forecast is an estimate, based upon current expectations and available information.

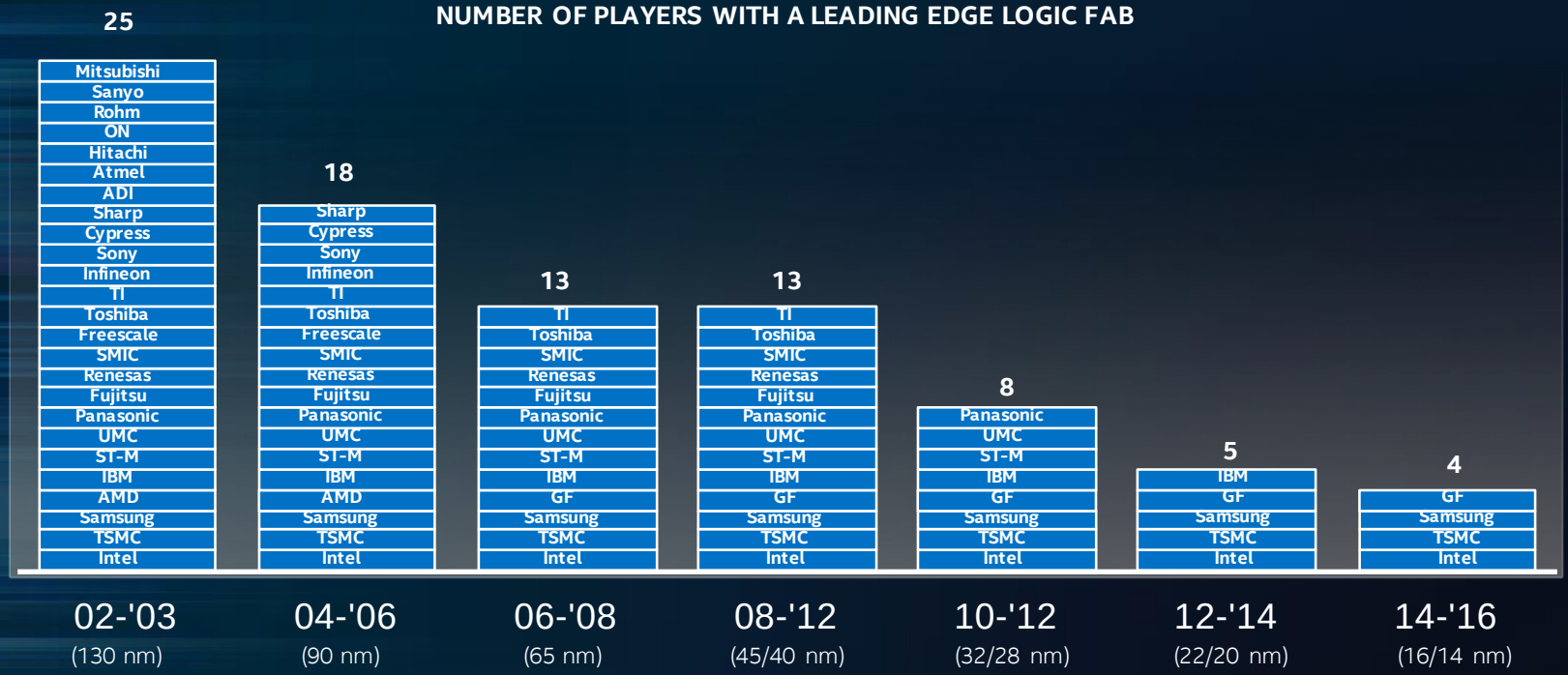
Source: Intel estimates.

OUR SCALE

INVESTMENT REQUIRED TO BUILD & EQUIP A LEADING EDGE WAFER FACTORY

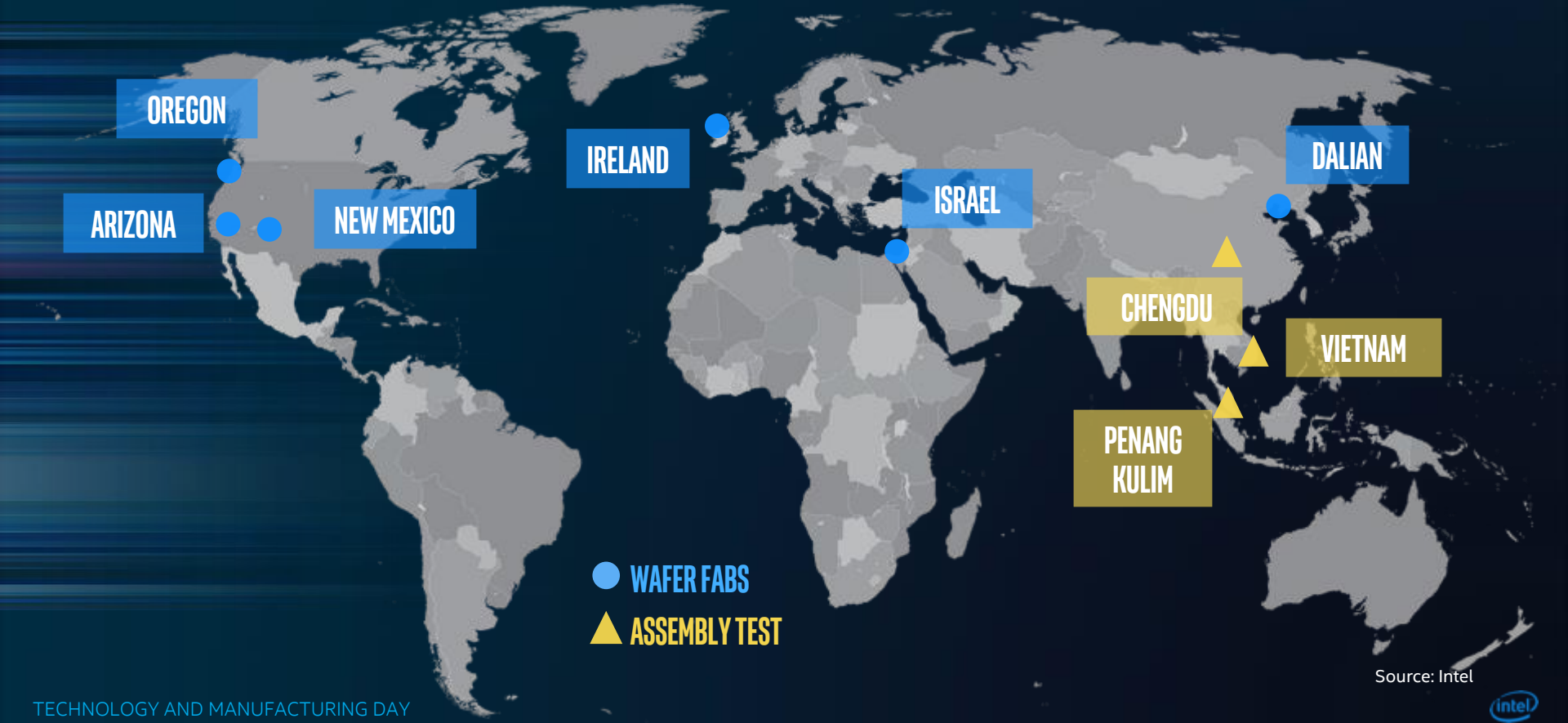
Source: Intel

SI TECHNOLOGY IS BECOMING RARE



Source: Amalgamation of analyst data and Intel analysis.

FAB AND ASSEMBLY TEST SITES



Source: Intel

GLOBAL MANUFACTURING BY THE NUMBERS

Source: Intel

UNITED STATES FOOTPRINT

US HIGH TECH JOBS

+50K

CONTRIBUTION TO US GDP

~$90B

$24B DIRECT
GDP CONTRIBUTION

LARGEST US HIGH-TECH CAPITAL INVESTOR

~$7B

ANNUAL AVERAGE
2011 – 2015

Over half of our high tech manufacturing jobs are in the US
80% of our revenue comes from outside the US

Source: Amalgamation of analyst data and Intel analysis.

WORLD CLASS SUPPLY CHAIN

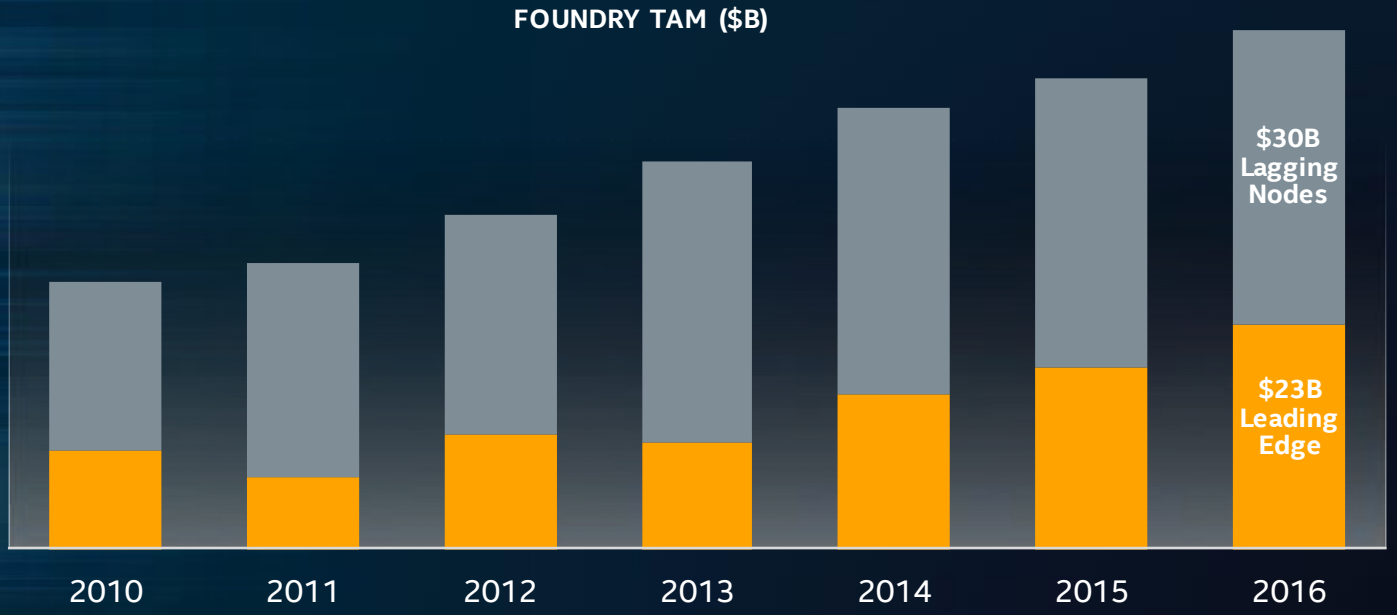
Gartner
Supply Chain Top 25

2016	
MASTER	Apple
MASTER	Proctor & Gamble
1.	Unilever
2.	McDonald's
3.	Amazon.com
4.	**Intel**
5.	H&M
6.	Inditex
7.	Cisco Systems
8.	Samsung Electronics
9.	The Coca-Cola Company
10.	Nestlé

Source: Gartner

INTEL CUSTOM FOUNDRY

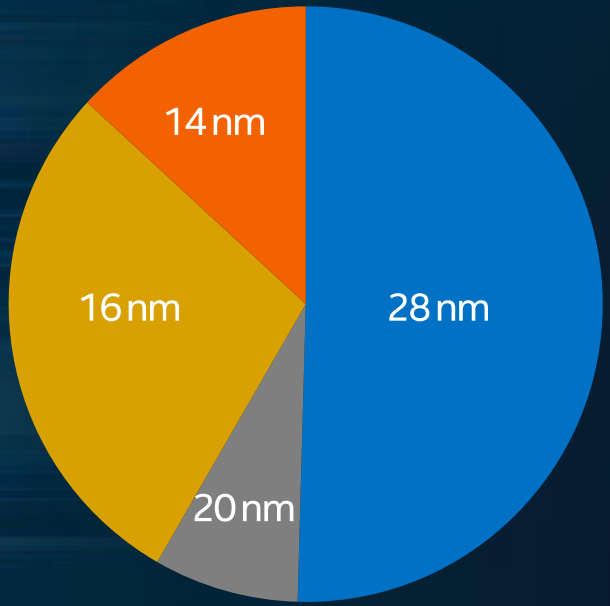
THE OPPORTUNITY ~ LEADING EDGE FOUNDRY MARKET IS GROWING



Note: Samsung and Intel internal are excluded from TAM. Leading edge defined as: 65nm and below for 2010, 45nm and below for 2011 and 2012, 32 nm and below for 2013-2016.
Source: Amalgamation of analyst data and Intel analysis.

2016 LEADING EDGE FOUNDRY MARKET

LEADING EDGE FOUNDRY TAM BY NODE



2016 TAM ($B)

$23B

GROWING AT 14%
(CAGR 2010 - 2016)

Note: Samsung and Intel internal are excluded from TAM. Leading edge defined as: 28 nm and below for 2016.
Source: Amalgamation of analyst data and Intel analysis.

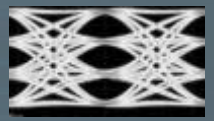
INTEL CUSTOM FOUNDRY

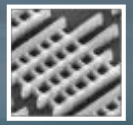
LEADERSHIP TECHNOLOGY & IP


Strained Silicon


FPGA


High-k Metal Gate


Optical & Serdes IP


FinFET Transistor


EMIB

ROBUST ECOSYSTEM

ANSYS
Mentor Graphics
arasan
Northwest Logic
Aricent
Open-Silicon
ARM
SANKALP semiconductor
asicNorth
SYNAPSE design
cadence
SYNOPSYS
Imagination
WIPRO

CO-OPTIMIZED PROCESSES IN CONJUNCTION WITH CUSTOMERS

Bringing tomorrow's technology today with comprehensive foundry services

INTEL CUSTOM FOUNDRY ~ ENABLING FINFET CAPABILITIES

1st gen FinFET technology focused on the networking market

2nd gen FinFET technology in mass production targeting networking, FPGA and mobile SOC markets

3rd gen FinFET technology, targeting high performance client and mobile markets

Proven Capability: Intel has manufactured ~7M FinFET wafers

INTRODUCING 22FFL PLATFORM

Extreme Integration Capability

Fast Time to Market

Cost Effective Design

FinFET for the masses

Ideal for highly integrated, cost sensitive products requiring a combination of high performance and ultra low power

PUTTING IT ALL TOGETHER

We continue to advance Moore's Law
resulting in significant product and cost benefits

We continue to outpace the rest of the industry
(~3 year lead on 14nm)

Our scale is a unique competitive advantage

We are building a foundry franchise

Source: Intel estimates

ONE MORE THING...

INTEL'S LEADERSHIP RESPONSIBILITIES

Addressing critical Sustainability and Human Rights issues

- Sourcing minerals responsibly
- Caring for the environment
- Promoting human rights programs
- Supply chain free of forced and bonded labor
- Reducing waste, water and carbon footprint

Inspiring employees, shareholders, customers